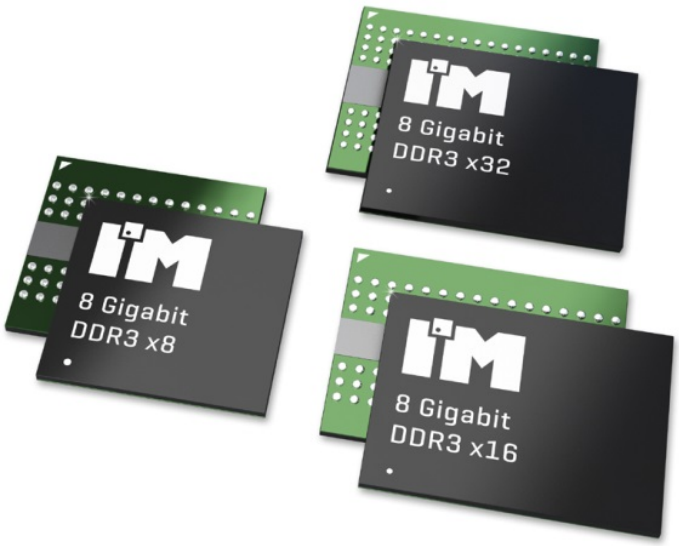
Doubling the DDR3 memory capacity to 8 Gigabit

The worldwide demand for memory capacity continues to grow. Industrial applications with soldered-down-DRAM often suffer from physical space constraints, resulting in a demand for high capacity memory-devices that fit in small spaces. Laptops, Desktop-PCs, Servers and embedded/industrial computers use memory modules, but often have only one to four sockets to upgrade with DDR3 DIMM or SO-DIMM modules.



Presently, the largest available density of monolithic DRAM components is 4 Gigabit in DDR3. For unbuffered DIMM and SO-DIMM modules based on 4 Gigabit DDR3 SDRAMs this results in a maximum module-capacity of 8 Gigabyte. Based on the current 30nm manufacturing process technology, a 4Gbit DRAM-die just fits into the standard package-dimensions for DDR3-components, which are FBGA78 or FBGA96.

With the next generation of 2x nm technology, DRAM manufacturers will be able to pack 8Gbit per monolithic DRAM die into similar package-dimensions as todays 4Gb components.

A die-stacking method known as a 'dual die package' (DDP) has become popular for memory-components over the last few years. DDP DRAMs combine two bare memory dies stacked inside one common chip-package. Separate control-lines for each die are connected to the balls of the FBGA-IC package. The assembled DDP chip is then accessible by the processor as if there were two separate components on the board, although both are inside one package.

In DDR3 technology, the memory is activated and selected by four control pins, which are connected from the memory-IC to the CPU. These contacts are named Chip-Select (CS), Clock-Enable (CKE), ZQ-calibration (ZQ) and On-Die-Termination (ODT).

A monolithic memory chip only has one set of these control-lines. In a DDP-chip however, two sets of control-lines are required. They are called CS0 and CS1, CKE0 and CKE1, ZQ0 and ZQ1, ODT0 and ODT1.

Application-designers who elect to use Dual-Die, dual chip-select DDR3 components on their products must prepare their board-layouts by routing the additional control-pins from every DRAM IC to the processor. They also need to watch that the I/O capacitance on the datalines is doubled as two dies share the same databus.

In reality, DDP-components are rarely utilized, because the special design-requirements prevent the usage of normal Single Chip-Select monolithic DRAMs as an alternate assembly.

Doubling the DDR3 memory capacity to 8 Gigabit

Yet another issue is that processors often lack the required number of DRAM control-lines to connect DDP chips, rendering it impossible to access further memory-ranks. Simply put, the existing 8 Gigabit DDP-solutions require too many special considerations that have prevented their widespread acceptance.

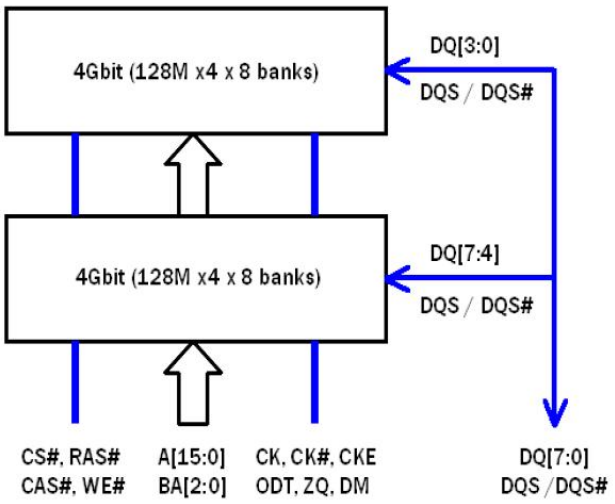
The Hong Kong based fabless company I'M Intelligent Memory has developed a unique way to manufacture 8 Gigabit DDR3 Single Chip-Select components with existing DRAM process-technologies.

The technology is based on a die-stack design very similar to conventional DDP components. The defining difference however, is that instead of two memory-dies being separately selectable, both are perfectly synchronized to work as a team, thereby creating a monolithic effect. For 8 Gigabit components with a x8 data-bus, each die contributes 4 data-lines while both share a common set of control lines. 8Gbit ICs with a x16 data-bus and Single-CS use two x8 dies inside.

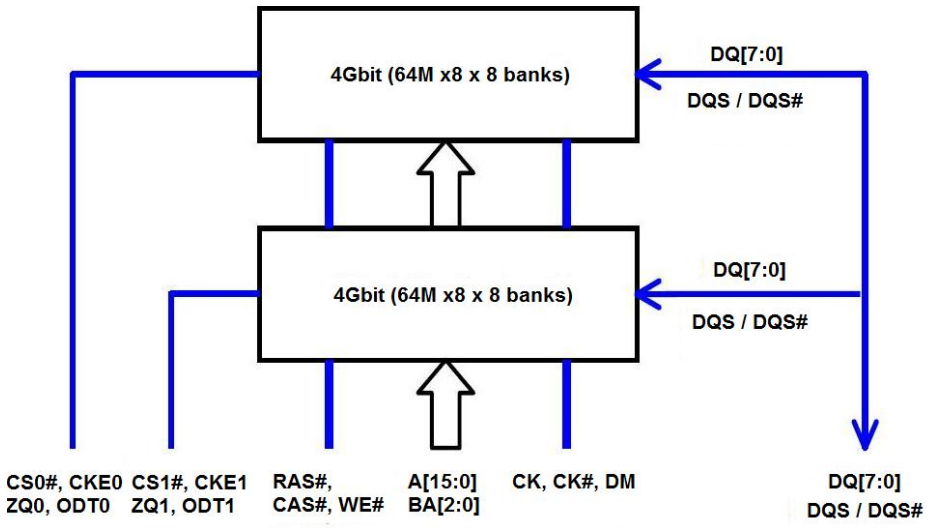
The end result then, is that the processor identifies both dies working together as a single, monolithic chip.

Example 1

I'M Intelligent Memory
8Gbit DDR3, x8
(128M x8 x 8 banks)
Single Chip-Select



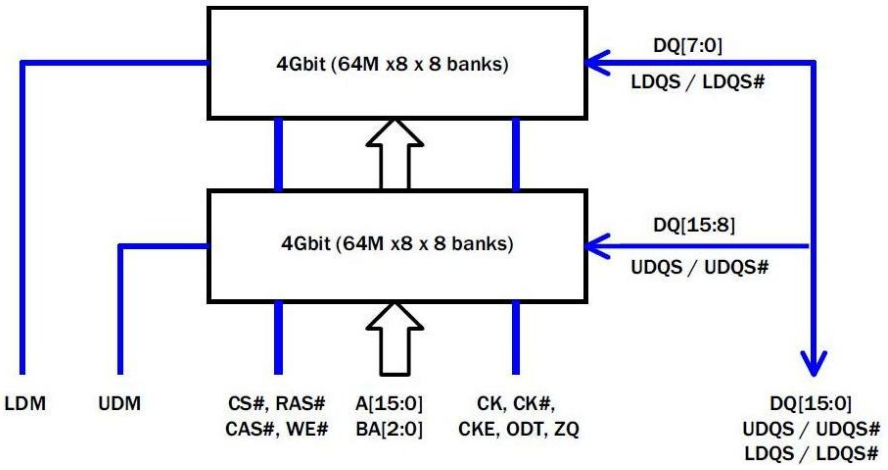
Conventional
8Gbit DDR3 DDP, x8
(64M x8 x 8 banks x 2 ranks)
with **two seperate sets of control lines**



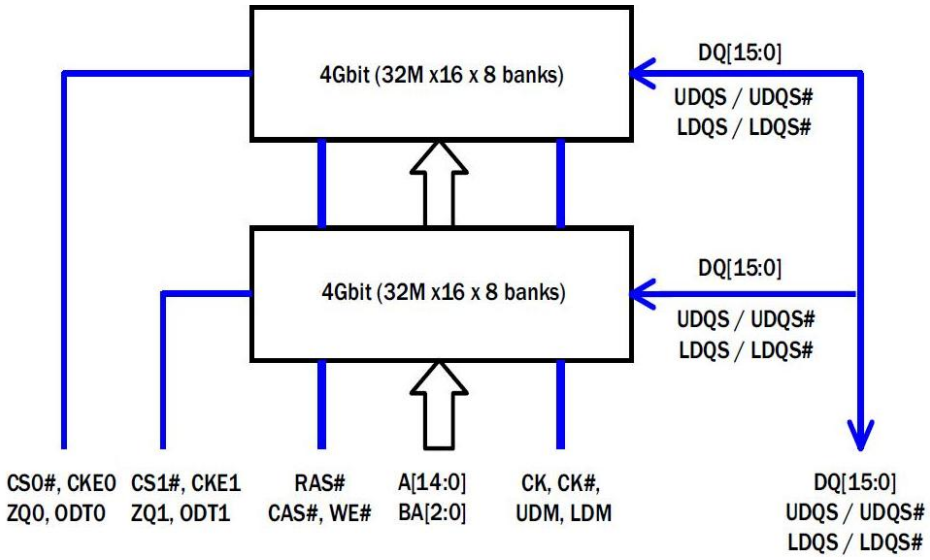
Doubling the DDR3 memory capacity to 8 Gigabit

Example 2

I'M Intelligent Memory
8Gbit DDR3, x16
(64M x16 x 8 banks)
Single Chip-Select



Conventional
8Gbit DDR3 DDP, x16
(32M x16 x 8 banks x 2 ranks)
with **two seperate sets of control lines**



I'M 8 Gbit Single-Chip-Select components come in JEDEC compatible packages of FBGA 78 for the x8 organization and FBGA 96 for the x16 version. The row/column/bank addressing of the 8 Gigabit components matches the specifications per JEDEC JESD79-3 for DDR3 products.

I'M Intelligent Memory 8Gb DDR3 SDRAM allow for new maximum levels of memory capacity without altering existing board-layouts or designs.

For more information
and to order samples, please visit
www.intelligentmemory.com