I'M ECC

DRAM with integrated error correcting code

A Revolutionary Product Family of Error-Correcting Memory for High Availability Applications

With a need to deliver highest quality products operating in all environments, cope with small and unique form-factors, all while containing costs, manufacturers of high-availability applications seek out solutions to accommodate this demand on their designs.

Complex systems always require a processor and memory. The long-term stability of the application depends upon the correct and consistent function of these key components at all times and under all conditions. The memory solutions presently deployed are typically one or multiple DRAM-ICs holding hundreds of millions, or even billions of data-bits of program code and essential data. If just one of these data-bits changes its value, it can cause incorrect calculations of algorithms, functional errors of the software or even system crashes.

Inside the DRAM, each data-bit is kept in very small capacitors charged with electrons that decide if the stored data-bit value will be a 0 or a 1. The structures of these capacitor-cells in the DRAM are extremely small and it is impossible to guarantee the identical quality of each of these cells. Throughout the 30 years history and continuous improvement of the process-technologies used to manufacture DRAMs, the consistency of the memory cell-quality has improved, but has yet to be perfected. There is still no comprehensive assurance of uniformity regarding the stability of each memory-cell within any given DRAM IC, not even on industrial or automotive graded memory-product.

The reality of this is devastating. A number of surveys and field-studies have been published on the likelihood and frequency of memory-errors. The most representative analysis has been performed by the University Of Toronto*, who examined the memory of the entire Google-Server-fleet for a period of 2 1/2 years. Although servers run under well-controlled environmental conditions, failure-rates counted in FIT (failure in time / per billion devices hours) of 25000 to 70000 FIT per Megabit were determined. Conversion into Gigabit and MTBF (mean time between failure) results in only 14 to 40 hours until the first bit flips in a standard 1 Gigabit DRAM chip as an average value.

The vast majority of memory errors found by the field-study were classified as single bit errors, or single-event-upsets (SEU), correctable by the Error-Correction-Code (ECC) functionality built into the server-processors. Such SEU's are typically non-permanent errors. Overwriting the incorrect memory-bit with correct data fixes the problem, but it can re-appear at any time in the same or another memory-cell.

I'M ECC PROTECTED

- on-chip ECC logic protects your data from single bit errors
- available in SDRAM, DDR1, Mobile DDR1, DDR2, DDR3, DDR4 and LPDDR4 technologies
- "plug-and-play" compatible to conventional JEDEC standard DRAM. No Hardware or Software modifications needed!
- industrial temperature as a standard, optional high temperature products for automotive and other applications

Upgrade any application to server-grade-reliability

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Small weaknesses of some memory cells or external disturbances like electromagnetic or particle radiation can cause unavoidable random bit-flips. The error-rate increase with the age and intense of use of the memory. In rare cases, a DRAM-cell can also get permanently damaged resulting in erratic data upon every access. While a system crash is undesirable in most applications, a bit-error that does not cause a crash may lend itself to even worse results. The error can linger in the system, cause incorrect calculations and multiply itself into further data. The corrupted data can then move to connected storage media and grow to an extent that may be difficult to recover. It is impossible for the customer or user to analyze the root-cause of such problems as they cannot be repeated. Most DRAM errors are transient and disappear after rebooting the system, while the caused damage stays. Manufacturers rarely see products returned from the field due to a presumed single-occasion memory-error.

In Servers and other high reliability environments, it has become common to protect the memory with an ECC algorithm adding a checksum stored with the data, allowing to correct single bit failures. This error-correction is implemented by widening the data-bus of the processor from 64 to 72 bits to accommodate an 8 Bit checksum with every 64 Bit word. Server processors are equipped with a logic to and from the extra-wide-memory. This logic generates ECC checksums and is able to verify and correct data read from the memory by these checksums.

Intelligent Memory (I'M) ECC DRAM components integrate error-correction logic with an internal spare memory-area for the checksums directly on the silicon of the DRAM IC itself. The memory performs the data-correction completely independent from the processor. When writing data to the ECC DRAM memory, the integrated logic automatically generates a checksum "on the fly" and stores it separately from the crucial data itself. Upon a Read from the DRAM, the checksum is used to verify the data and correct it when required. The complete process of error-correction runs without any noticeable delays or latencies and does not require any specific hardware or software changes. The processor does not need to have ECC capabilities. I'M ECC DRAMs are direct drop-in replacements for any conventional, unprotected JEDEC standard DRAM, making them the most simple and effective way to improve memory reliability and stability to server-grade level by adding error-correction.

Nearly all electronic products can benefit from I'M ECC memory. Any application requiring consistent system-availability and stability for days, months and years should consider to add ECC protection. But also for applications that require the highest quality, reliability and functional safety, or run in the harshest of environments, a memory error protection is mandatory. Networking devices like routers or access points are expected to be always on and ready to use. Control-systems, industrial computers, harddisk-drives, security systems, medical devices, automotive, avionic and space based electronics need to ensure system and operational stability as well as long term functionality.

I'M ECC DRAM products provide the ability to elevate thousands of applications to new levels of memory reliability.

Available in all common memory technologies

I'M ECC DRAMs will be available in the standard memory technologies available in SDRAM, DDR1, Mobile DDR1, DDR2, DDR3, DDR4 and LPDDR4. Capacities range from 512 Megabit devices up to 2 Gigabit and the parts are available in all common bit-widths like x8, x16 or even x32.

Simply "plug-and-play" compatible

All I'M ECC DRAMs are fit/form/function compatible to conventional JEDEC Standard DRAMs, same package, same pinout, same signals and timings. No performance losses, no delays and most important: Neither software nor hardware modifications are required!

By replacing the normal memory-components with I'M ECC DRAMs, your application will immediately take benefit of a multiple million times higher reliability.

Stronger than standard error-correction

While on Servers, one bit out of each 72 Bit word can be corrected, the ECC DRAMs correct the data per chip. If 8 chips in a x8 organization are required to fit the 64 Bit processor-databus, each of these 8 Chips will detect and correct single bit errors. The more I'M ECC DRAMs are running in parallel on the processors databus, the stronger is the grade of the ECC protection.

Optional eXtra robustness

For all those who cannot get enough of the term quality, we have an advanced version of I'M ECC DRAM - I'M XR ECC DRAM. The "eXtra Robustness" XR ECC DRAMs add a physical protection to the stored data-bits by holding the bits in larger capacitors, with a redundant data topology. This larger electric charge and redundant topology used to store the data-bit reduces the impact of typical DRAM cell leakage effects, thus leads to a significant higher robustness, safer data structure and data-retention capabilities.

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Increase your sales by showing the reliability of your application

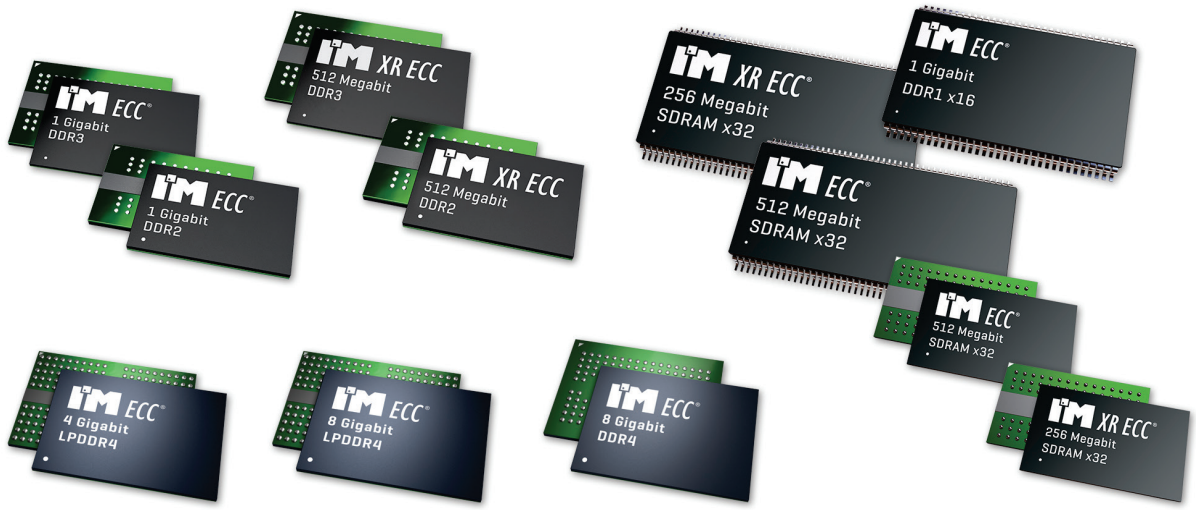
Customers using the Intelligent Memory ECC DRAMs may use the "I'M ECC protected" seal to promote their products. Put this seal on your website, attach it as a sticker right onto your product, use the logo for your product presentations and show your customers how your applications distinguish themselves from the competition in terms of quality, reliability and robustness.

References

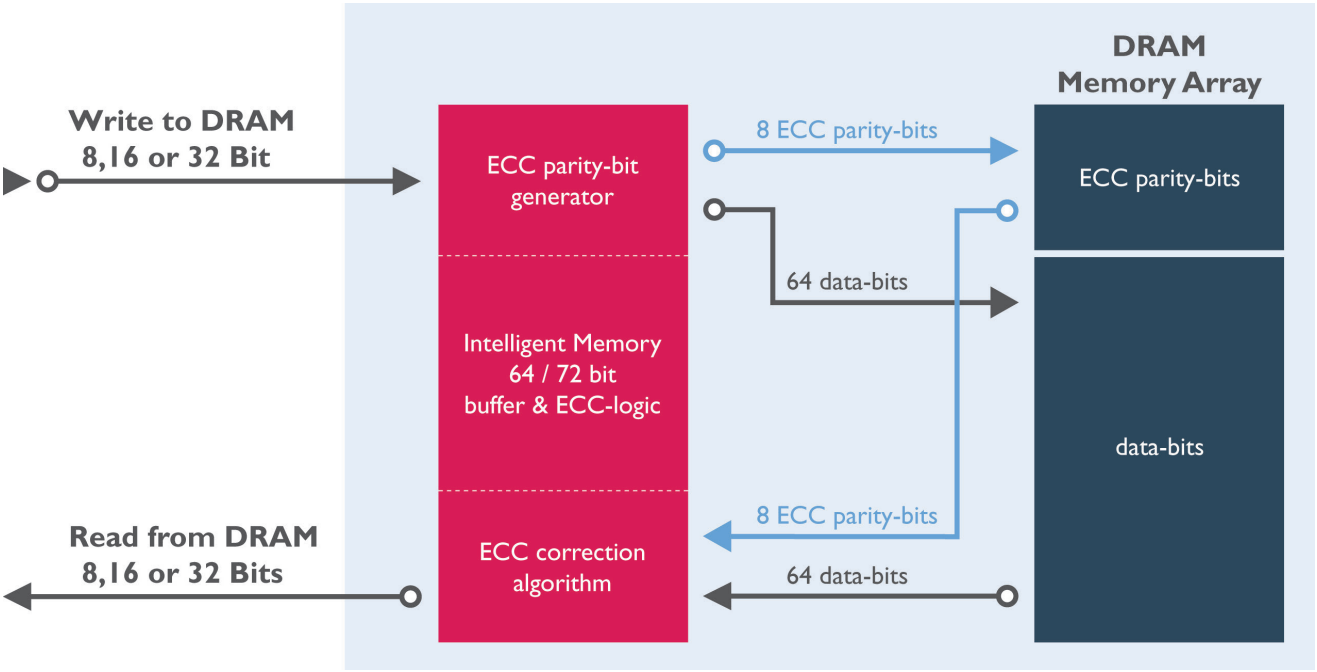
B. Schroeder, et al. DRAM errors in the wild: A large-scale field study. In SIGMETRICS, 2009.

Pinheiro, Eduardo - Google Inc., Mountain View, CA

Weber, Wolf-Dietrich - Google Inc., Mountain View, CA



I´M ECC - functional block diagram



I'M ECC –DRAM with integrated error correcting code

Product Family Overview

I'M ECC DRAM with integrated error correction

Technology	Capacities	Organizations	Voltage options	Package	Speed Options
LPDDR4	4Gbit, 8Gbit	x16, x32	1.1V	FBGA200	LPDDR4-2400/3200
DDR4	8Gbit	x16, x32	1.2V	FBGA144	DDR4-2133/2400/2666/2933/3200
DDR3	1Gbit	x8, x16	1.5V	FBGA78 (x8), FBGA96 (x16)	DDR3-1333/1600
DDR2	1Gbit	x8, x16	1.8V	FBGA60 (x8), FBGA84 (x16)	DDR2-667/800
DDR1	1Gbit	x8, x16	2.5V	FBGA60, TSOP66	DDR-333/400
Mobile DDR	1Gbit	x16	1.8V	FBGA60	DDR-333/400
SDRAM	512Mbit	x8, x16, x32	3.3V	TSOP54 (x16 x8), FBGA90, TSOP86 (x32)	PC-133/166

eXtra-Robust I'M ECC DRAM with integrated error correction

Technology	Capacities	Organizations	Voltage options	Package	Speed Options
DDR3	512Mbit	x8, x16	1.5V	FBGA78 (x8), FBGA96 (x16)	DDR3-1333/1600
DDR2	512Mbit	x8, x16	1.8V	FBGA60 (x8), FBGA84 (x16)	DDR2-667/800
DDR1	512Mbit	x8, x16	2.5V	FBGA60	DDR-333/400
Mobile DDR	512Mbit	x16	1.8V	FBGA60	DDR-333/400
SDRAM	256Mbit	x32	3.3V	FBGA90 TSOP86	PC-133/166

Part No. Decoder

IM E 1G 08 D3 E E B G - 15 I A

Intelligent Memory

E = integrated ECC
R = eXtra Robustness
X = eXtra Robustness + integrated ECC

IC Capacity

51 = 512 Megabit
1G = 1 Gigabit
2G = 2 Gigabit
4G = 4 Gigabit
8G = 8 Gigabit
AG = 16 Gigabit

DRAM I/O width

08 = x8
16 = x16
32 = x32

Memory Type

SD = SDRAM
D1 = DDR1
MD = Mobile DDR
D2 = DDR2
D3 = DDR3
D4 = DDR4
L4 = LPDDR4

Voltage

B = 3.3V (SDRAM)
C = 2.5V (DDR1)
D = 1.8V (DDR2)
D = 1.8V (mobile DI
E = 1.5V (DDR3)
G = 1.2V (DDR4)
H = 1.1V (LPDDR)

IC Revision

A = Revision A
B = Revision B
etc.

Package

B = FBGA
T = TSOP
D = FBGA DDP (2 seperate Chip-Select lines)
Q = FBGA QDP (4 seperate Chip Select lines)

Speed Grade

75 = SDRAM-133 CL3 or 100MHz CL2
75 = DDR1-266 CL2.5 (also for Mobile DDR)
6 = DDR1-333 CL2.5 (also for Mobile DDR)
3 = DDR2-667 CL5-5-5
25 = DDR2-800 CL5-5-5
15E = DDR3-1333 CL9-9-9
053 = LPDDR4-3777
062 = DDR4-3200 CL22-22-22 also LPDDR4-3200
068 = DDR4-2933 CL21-21-21
075 = DDR4-2666 CL19-19-19
083 = DDR4-2400 CL17-17-17 also LPDDR4-2400

Temperature range

For SDRAM, DDR1 and Mobile DDR:
Blank = Commercial Temperature 0°C to +70°C Ta
I = Industrial Temperature -40°C to +85°C Ta
H = High Temperature -40°C to +105°C Ta and +115°C Tcase(MAX)
X / Y = Extreme Temperature:
X = X-Temp -40°C to +125°C Ta and +135°C Tcase(MAX)
Y = Y-Temp -40°C to +125°C Ta and +135°C Tcase(MAX)
Note: For Y-Temp, the refresh rate must be doubled when the Tcase exceeds 105°C

For DDR2, DDR3, DDR4, LPDDR:
Blank = Commercial Temperature 0°C to +95°C Tcase
I = Industrial Temperature -40°C to +95°C Tcase
H = High Temperature -40°C to +105°C Tcase
X / Y = Extreme Temperature:
X = X-Temp -40°C to +125°C Tcase
Y = Y-Temp -40°C to +125°C Tcase
Note: For Y-Temp, the refresh rate must be doubled when the Tcase exceeds 105°C

Automotive (AEC-Q100) Option

Blank = Standard Grade
A = Automotive Grade (AEC-Q100)

RoHS compliance

G = Green / RoHS
Blank = Leaded