DRAM 101

EBOOK

Chapter 1
DRAM Basics

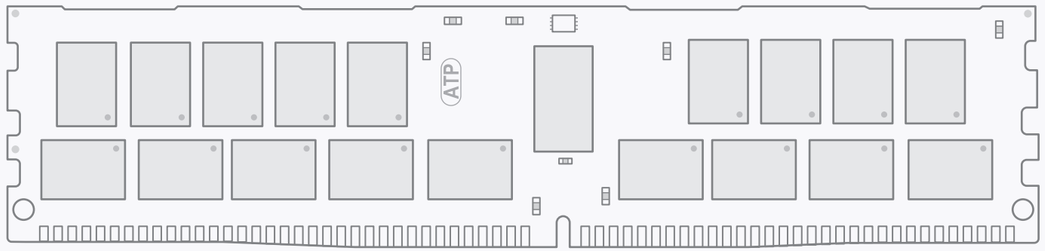
Dynamic Random-Access Memory (DRAM) Overview

What is Dynamic Random-Access Memory?

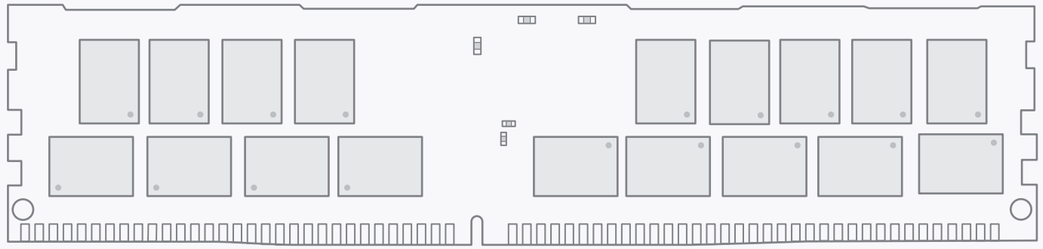
DRAM is the hardware in a computer that temporarily stores the operating system (OS), application programs, and working data currently in use.

- It is also known as “main” or “short-term” memory.
- “Random” means data can be accessed (read and changed) directly and in any order.

DRAM is installed on the motherboard’s memory slots as dual inline memory modules (DIMMs).
DIMMs are called as such because they have two independent rows of pins in front and at the back.



Front



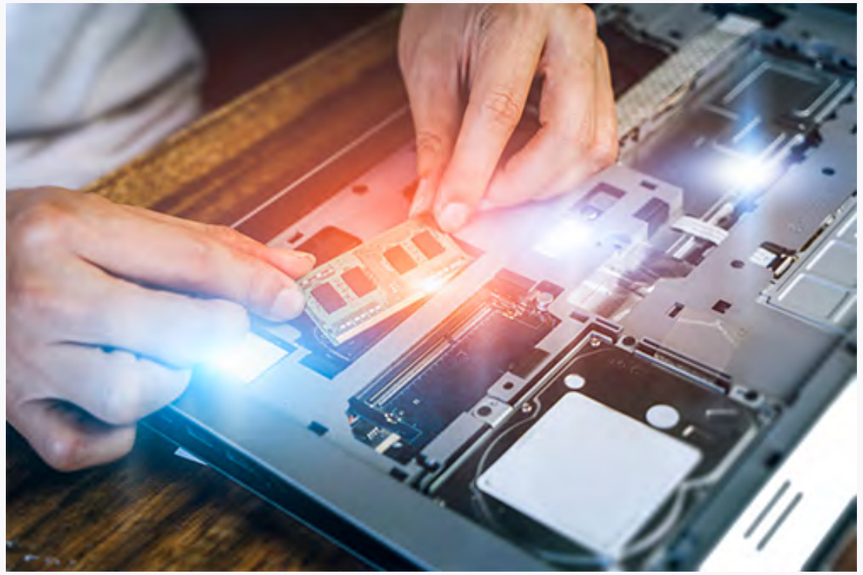
Back

Main Types of RAM

There are two main types of RAM: Dynamic RAM (DRAM) and Static RAM (SRAM).

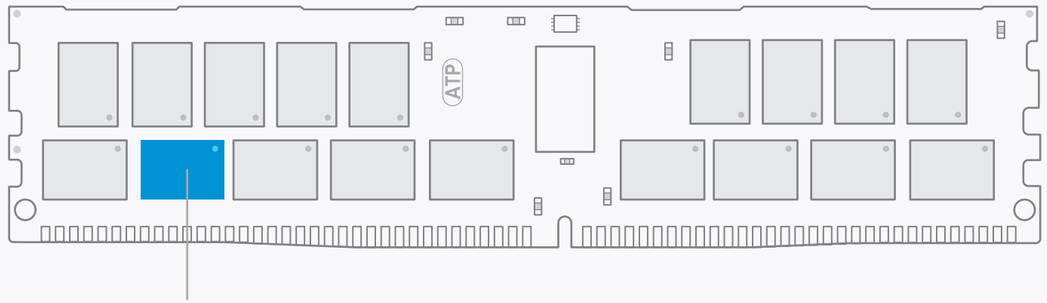
- **DRAM (pronounced DEE-RAM)**, is widely used as a computer's main memory. Each DRAM memory cell is made up of a transistor and a capacitor within an integrated circuit, and a data bit is stored in the capacitor. Since transistors always leak a small amount, the capacitors will slowly discharge, causing information stored in it to drain; hence, DRAM has to be refreshed (given a new electronic charge) every few milliseconds to retain data.

- **SRAM (pronounced ES-RAM)**, is made up of four to six transistors. It keeps data in the memory as long as power is supplied to the system unlike DRAM, which has to be refreshed periodically. As such, SRAM is faster but also more expensive, making DRAM the more prevalent memory in computer systems.



How DRAM Stores Data

There are two main types of RAM: Dynamic RAM (DRAM) and Static RAM (SRAM).



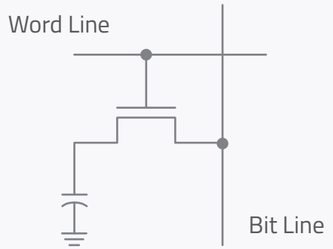
A **memory chip** is made up of transistors and capacitors, which are paired to form a memory cell.

DRAM stores each bit of data in a capacitor within an integrated circuit (IC). The capacitor can either be charged or discharged, representing the two values of a bit: 0 and 1.

The transistor acts a switch, allowing the memory chip controller to read the capacitor or change its state.

Bit

The term “bit” is short for binary digit. As the name suggests a bit represents a single digit in a binary number. A bit is the smallest unit of information used in computing system and can have a value of either “ 1 “ or “ 0 “.

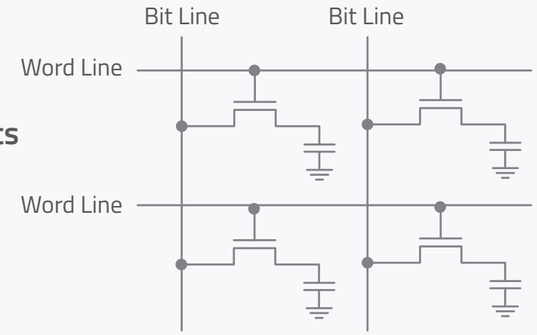


Cell

Byte

A byte consists of 8 bits. Almost all specifications of computer’s capabilities are represented in bytes.

1 Byte = 8 bits

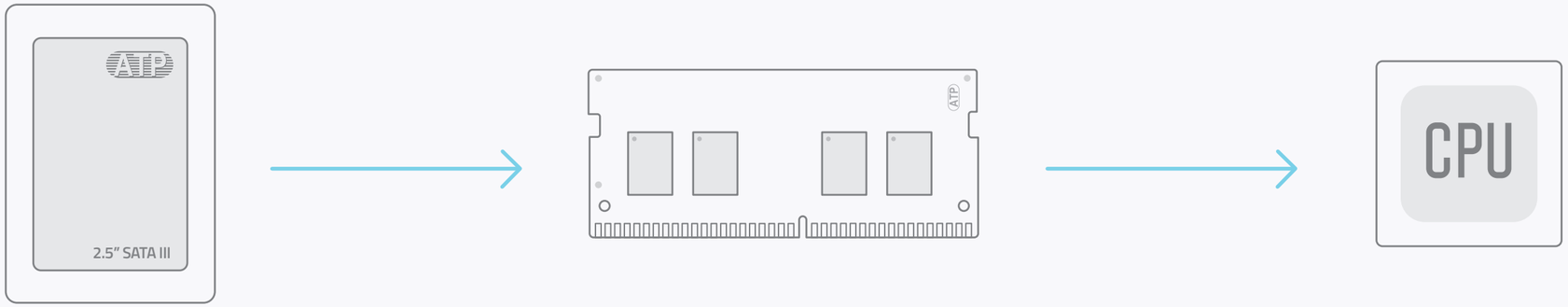


Array

Volatile vs. Non-Volatile Memory

VOLATILE	NON-VOLATILE
Internal/Main/Primary memory	External/Secondary memory
Loses data quickly when power is removed	Data remains stored even if power is removed
Temporary/short-term storage	Permanent/long-term storage
Faster	Slower
Less storage capacity	Generally, has more storage capacity
Impacts system performance	Impacts storage capacity
CPU can directly access data	CPU cannot directly access data
Installed on the motherboard memory slots	May be removable, or embedded/ soldered on the motherboard

Basic Function of DRAM



Data or program is first stored on non-volatile media, such as a solid state drive (SSD).

The data or program is loaded into the DRAM.

The processor can then access the data or run the program.

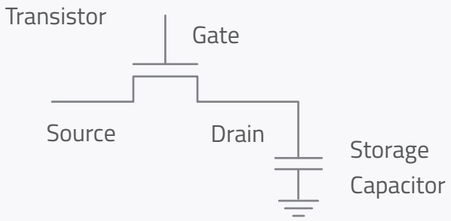
If DRAM capacity is too low, it may not be able to hold all the data or programs that the CPU needs, so the RAM keeps going back to the SSD, thus slowing down performance.

DRAM IC Architecture

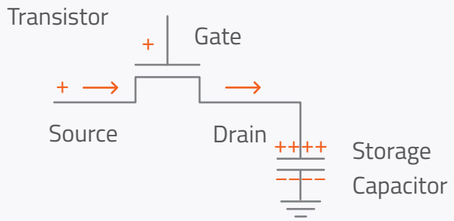
Memory Cell

Charge & Discharge

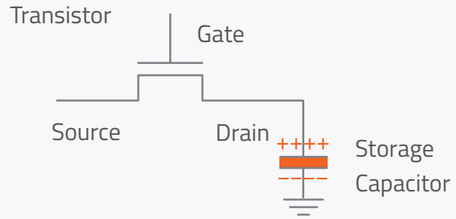
- DRAM stores each bit of data in a separate capacitor within an integrated circuit.
- The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1.
- Volatile memory: requires power to maintain the stored information.



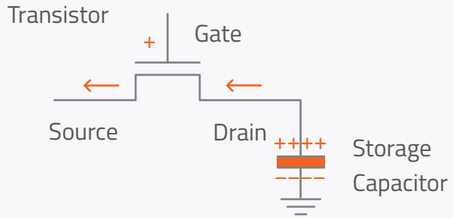
One Memory Cell



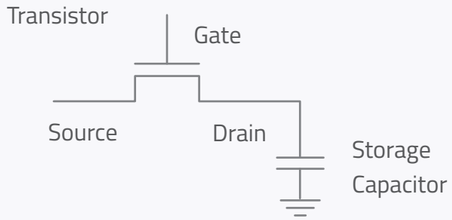
Charging



Charged: Represented as “1”



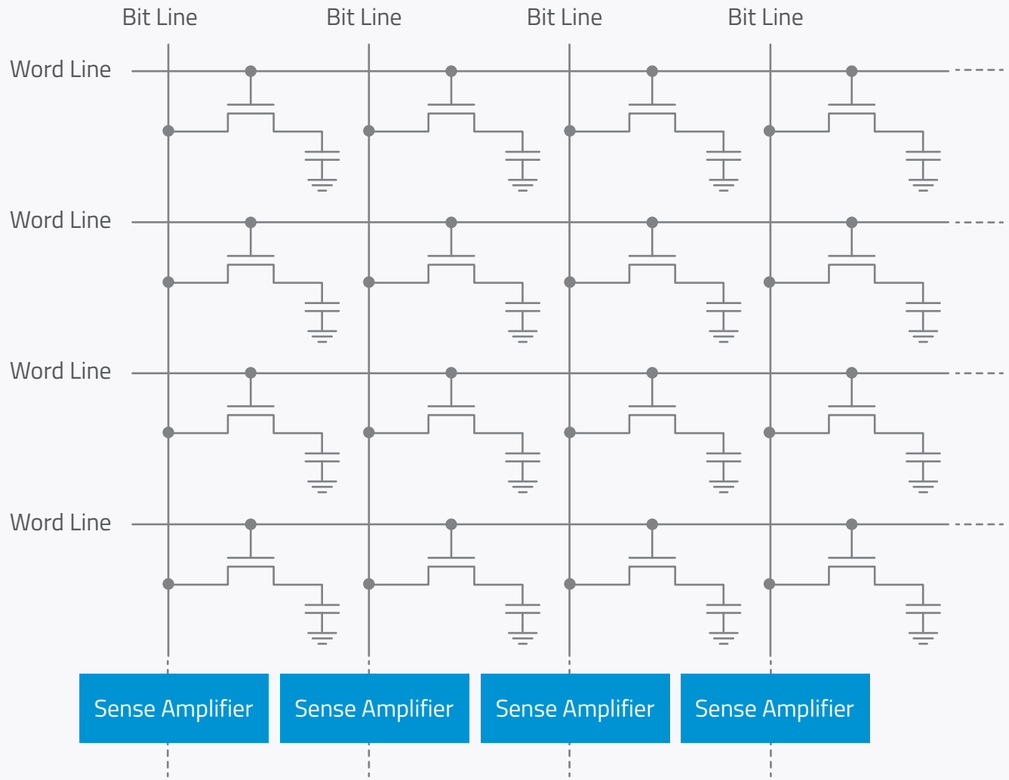
Discharging



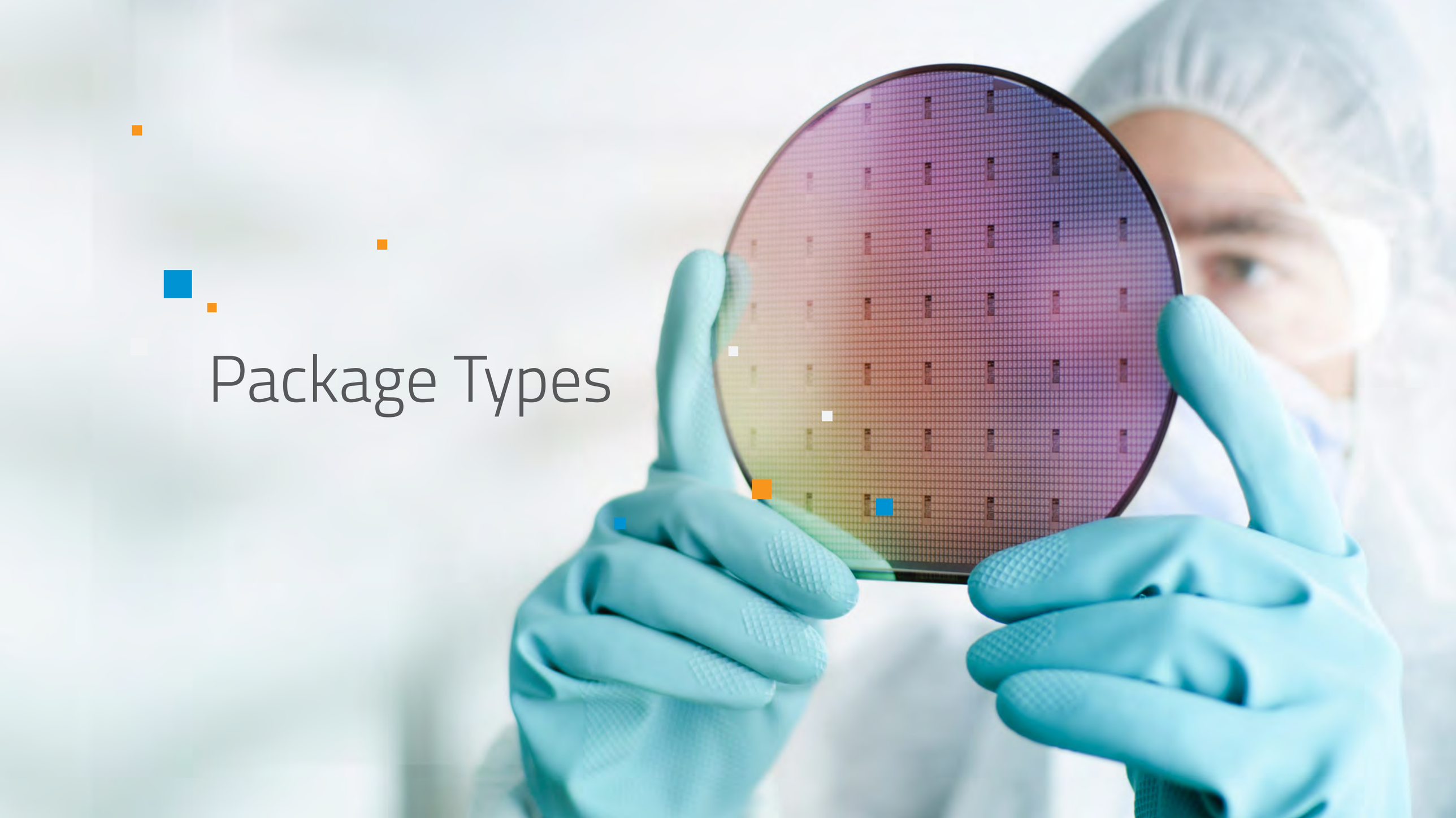
Discharged: Represented as “0”

Memory Cell Array

- The memory cells are arranged in a two-dimensional array connected by **word line** and **bit lines**.
- **Differential Sense Amplifiers** are connected to each bit line.
  - Compare the new bit line voltages with the original voltages.
  - Temporarily store the voltages values read from the cell in the flip-flop latch circuitry.
  - Output one of the values to data bus.



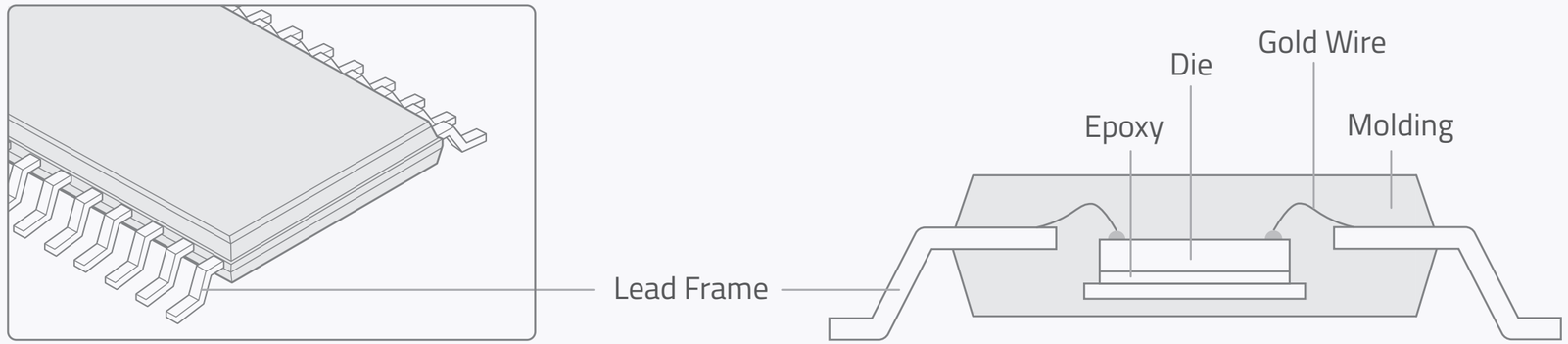
Package Types



Package Types

TSOP (Thin Small Outline Package)

TSOP is a type of surface mount packaging for integrated circuits (IC). It has a very thin and low profile and tight lead spacing. It is rectangular in shape and comes in two configurations: TSOP1 has the leads on the ends or short edges of the package while TSOP2 has the leads on the sides or long edges of the package. The pins have an “L” shape (“gull-wing leads” according to JEDEC) and the package is typically made of plastic and ceramic.



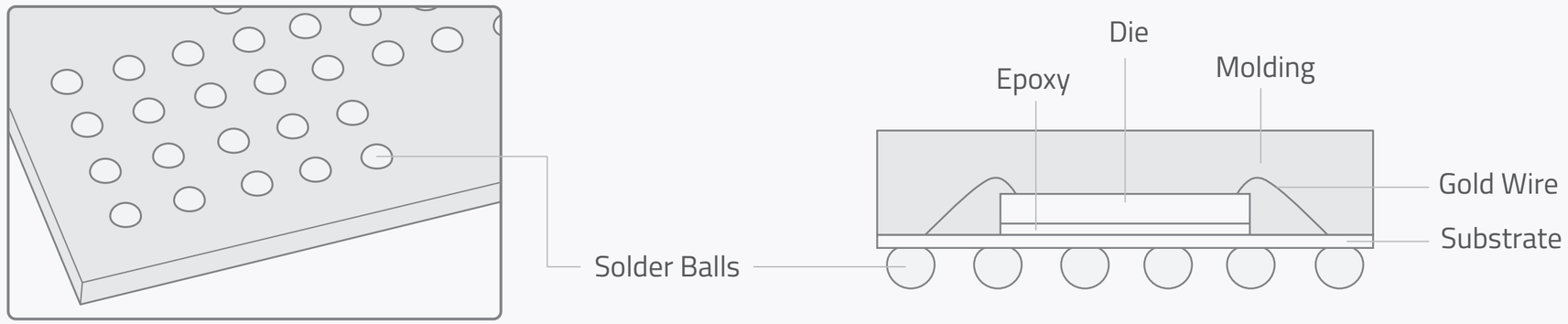
TSOP is used on ATP SDRAM/DDR modules.

Package Types

BGA (Ball Grid Array)

BGA is a type of surface mount packaging for integrated circuits (IC). It uses a grid of solder balls attached to the substrate. The entire bottom surface is used and not just the perimeter, hence providing more interconnection pins. The leads to the balls are also shorter, enabling better performance at faster speeds.

- The transition from TSOP to BGA happened around DDR1 to fit into the small outline PCB by maximum density per IC quantity, especially for high-density SO-DIMM.
- Main benefit: The thermal specification Ta (ambient) of the DRAM module increased from 70°C to 85°C, since the BGA design allows better heat conduction between the IC package and PCB, preventing the chip from overheating.

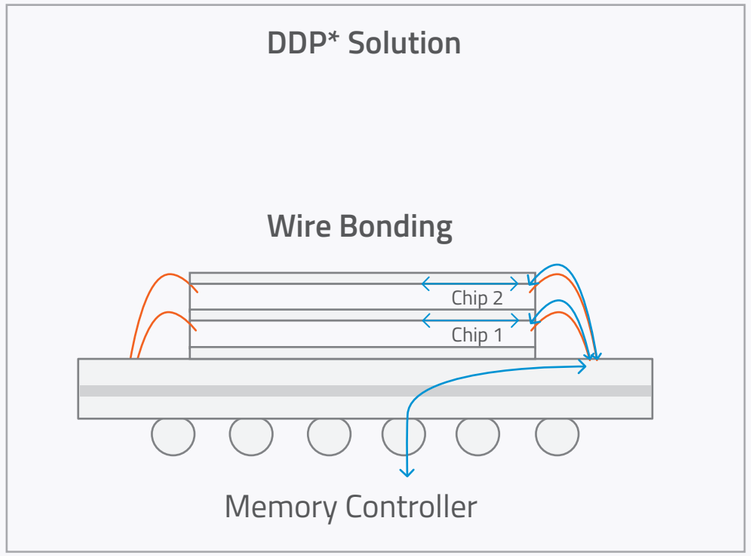


BGA package is used on ATP DDR1/2/3/4/5, SDP*, DDP* and TSV*.

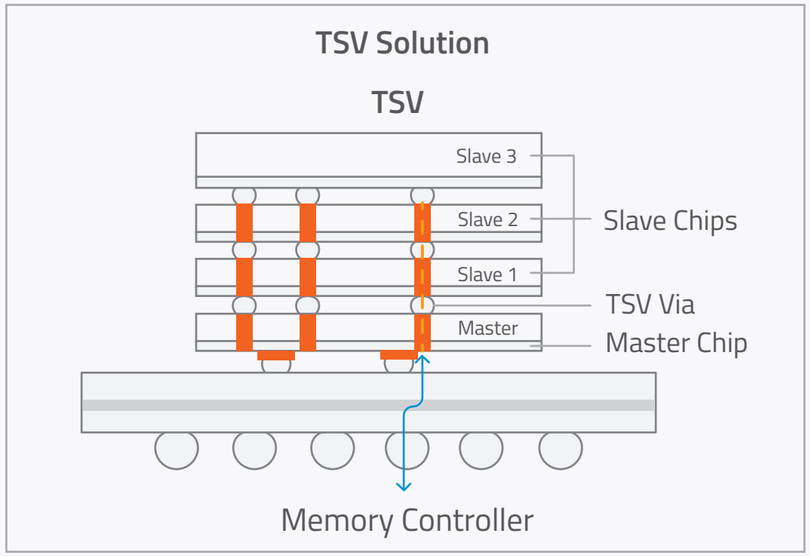
* SDP: Single-Die Package
DDP: Dual-Die Package
TSV: Through-Silicon Vias

Stacking Technologies to Increase Density

A DRAM IC may have multiple stacks of memory dies to increase density. Stacking is used only for module configurations that absolutely need the increased densities that single-die packaging (SDP) cannot support. The following illustrations show conventional DDP* solution with wire bonding methods and Through Silicon Via (TSV) technology solution.



BGA DDP* Solution: DDR3/DDR4/DDR5 modules



Through-Silicon Vias 3-Dimensional Stacking (TSV 3DS) Solution —3DS, 4H, 8H: DDR4/DDR5 modules**

Only the Master chip communicates with the Memory Controller regardless of the stacking.

TSV Advantages:

- Higher density
- Better data transfer rate
- Reduces interconnect delay
- Better signal integrity and performance
- Lower power consumption

* DDP: Dual-Die Package

** 4H, 8H: Refers to die stacking height

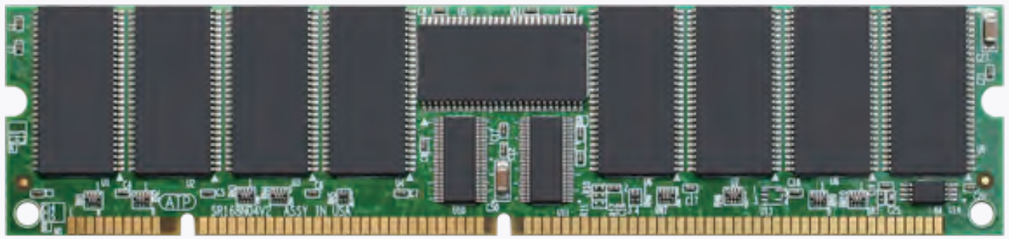
Generations

Legacy SDRAM: SDR vs. DDR

Synchronous Dynamic Random-Access Memory (SDRAM) refers to memory that operates synchronously with the system clock. The synchronous interface enables the SDRAM to operate in a more complex fashion and at much higher speeds than an asynchronous DRAM.

- **Single Data Rate (SDR) SDRAM**

  Also simply known as SDRAM, it transmits data (read/write) on only one clock transition, typically on the clock's rising edge, hence the name single data rate. To perform another operation, it has to wait for the previous one to be completed, making it slower than succeeding SDRAM generations.



ATP SDRAM module

- **Double Data Rate (DDR) SDRAM**

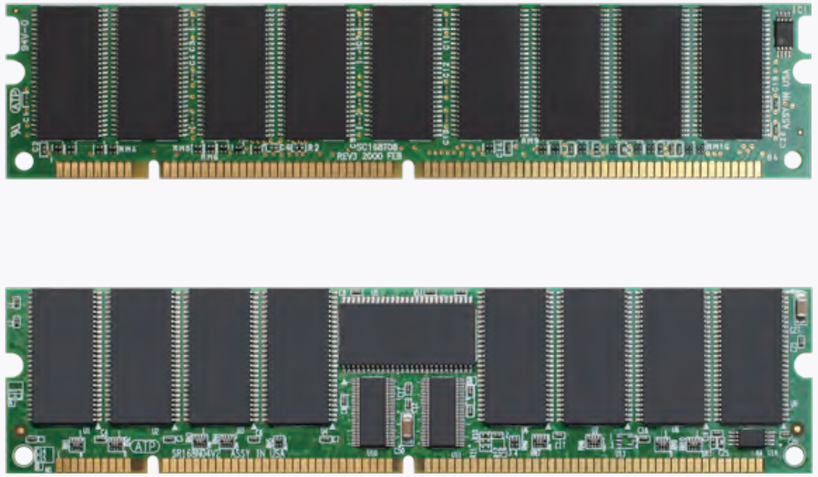
  Also simply known as DDR, it achieves greater bandwidth and faster performance at twice the speed of SDR by transferring data on both the rising and falling edges of a clock cycle.

  DDR generations, which will be discussed in succeeding sections, include:
  - DDR1
  - DDR2
  - DDR3
  - DDR4
  - DDR5

ATP Legacy SDRAM Specifications

Synchronous Dynamic Random-Access Memory (SDRAM) refers to memory that operates synchronously with the system clock. The synchronous interface enables the SDRAM to operate in a more complex fashion and at much higher speeds than an asynchronous DRAM.

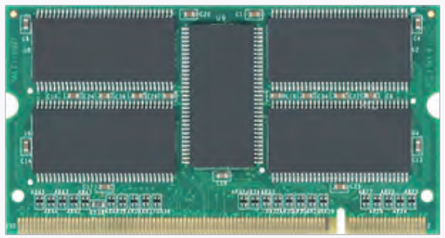
SDRAM	
DIMM Type	Non-ECC SO-DIMM
Density	64 MB to 256 MB
Speed up to (MT/s)	133
PCB Height	Low Profile
Operating Temperature (Ta)	0°C to 70°C



Please refer to motherboard/CPU/chipset documentation for memory requirements and compatibility.

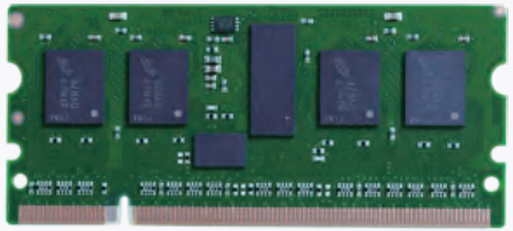
ATP Legacy DDR1 Specifications

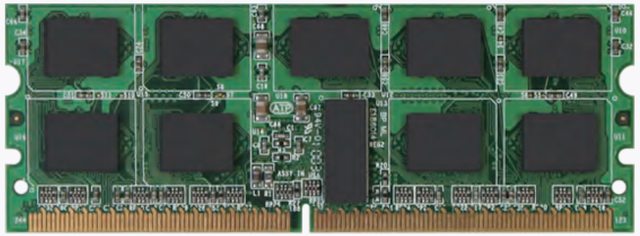
DDR1		
DIMM Type	Non-ECC UDIMM	Non-ECC SO-DIMM
Density	256 MB	128 MB to 512 MB / 1 GB
Speed up to (MT/s)	400	400
PCB Height	Low Profile	Low Profile
Operating Temperature (Ta)	0°C to 70°C	0°C to 70°C / -40°C to 85°C



Please refer to motherboard/CPU/chipset documentation for memory requirements and compatibility.

ATP Legacy DDR2 Specifications





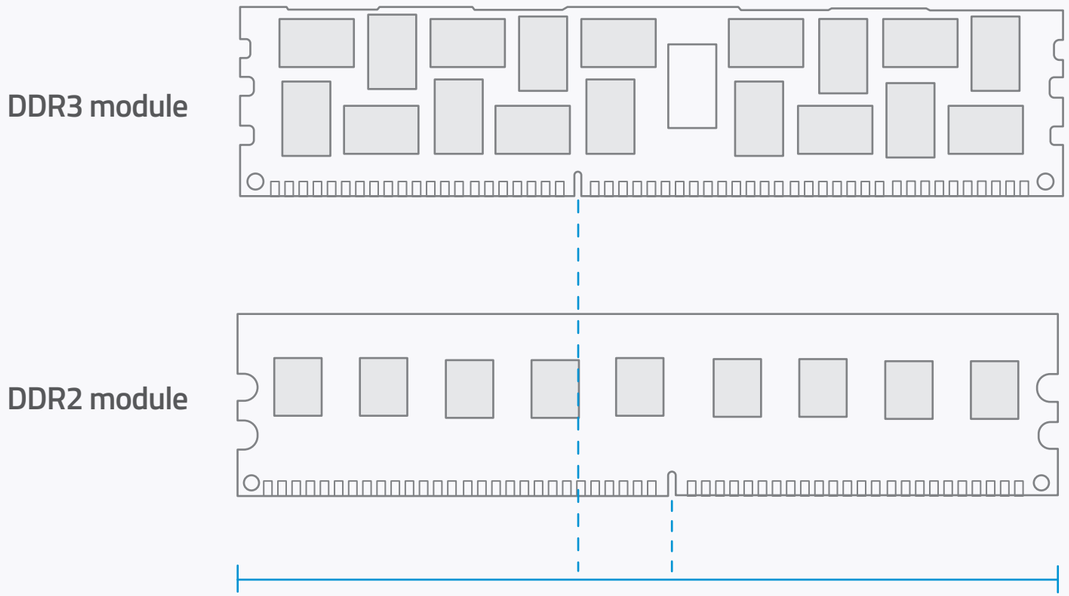
DDR2			
DIMM Type	ECC UDIMM	Non-ECC UDIMM	Non-ECC SO-DIMM
Density	1 GB to 2 GB	1 GB to 2 GB	256 MB / 1 GB to 4 GB
Speed up to (MT/s)	800	800	800
PCB Height	Low Profile	Low Profile	Low Profile
Operating Temperature (Ta)	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C

Please refer to motherboard/CPU/chipset documentation for memory requirements and compatibility.

DDR3

DDR3 operates at 1.5V (normal) and 1.35V (low voltage), consuming less power than its predecessors, and delivers better performance with a transfer speed of up to 1866 MT/s.

A DDR3 module is not pin-compatible with prior-generation modules and its alignment key is located differently to prevent being inserted into incompatible slots.



ATP DDR3 Specifications

DDR3							
DIMM Type	RDIMM	ECC UDIMM	Non-ECC UDIMM	ECC SO-DIMM	Non-ECC SO-DIMM	Mini-RDIMM	Mini-UDIMM
Density	1 GB to 32 GB	1 GB to 16 GB	1 GB to 16 GB	1 GB to 16 GB	1 GB to 16 GB	1 GB to 16 GB	1 GB to 16 GB
Speed up to (MT/s)	1866	1866	1866	1866	1866	1600	1600
PCB Height*	Low profile / VLP / ULP	Low profile / VLP / ULP	Low profile / VLP / ULP	Low Profile	Low Profile	Low profile / VLP / ULP	Low profile / VLP / ULP
Operating Temperature (Ta)	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C

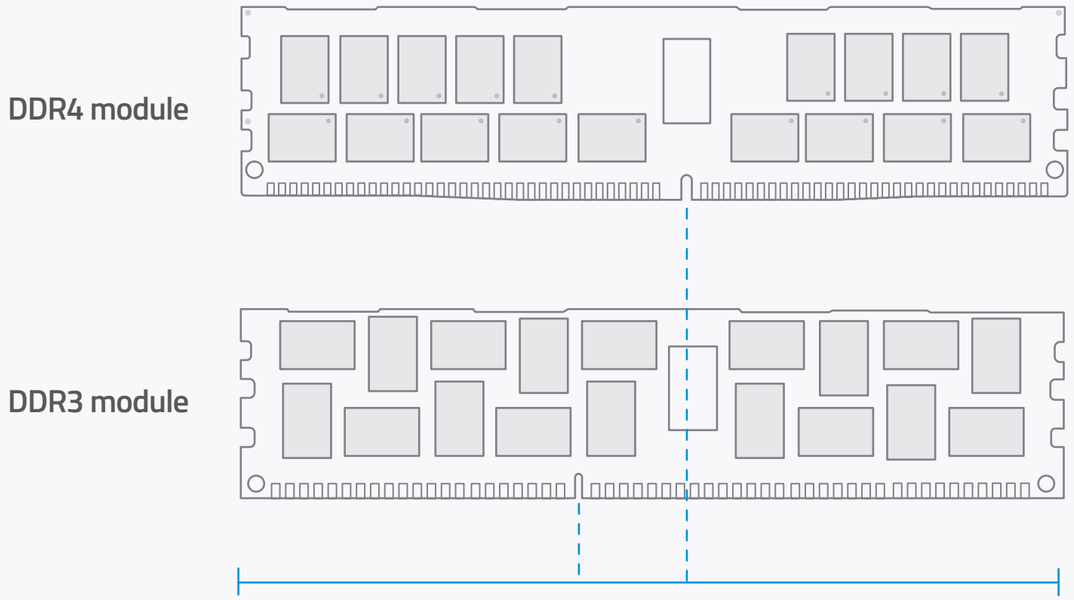
* VLP: 0.74", ULP: below 0.74"

Please refer to motherboard/CPU/chipset documentation for memory requirements and compatibility.

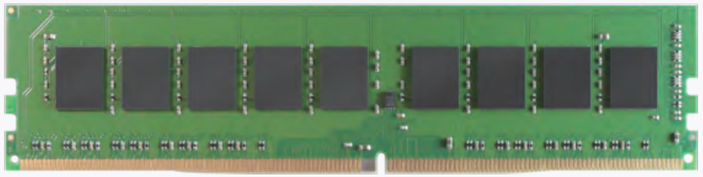
DDR4

DDR4 is the evolutionary transition from DDR3. It consumes a mere 1.2V while performing up to 3200 MT/s data transfer rate to deliver faster performance while generating more power savings over earlier DRAM technologies.

A DDR4 module has 288 pins (260 pins for SO-DIMMs) and is not pin-compatible with prior-generation modules. The edge connector looks like a slightly curved “V” to facilitate insertion. This design also lowers insertion force, as not all pins are engaged at the same time during module insertion. Its alignment key is located differently to prevent being inserted into incompatible slots.



ATP DDR4 Specifications



DDR4							
DIMM Type	RDIMM	ECC UDIMM	Non-ECC UDIMM	ECC SO-DIMM	Non-ECC SO-DIMM	Mini-RDIMM	Mini-UDIMM
Density	4 GB to 128 GB	4 GB to 32 GB	2 GB to 32 GB	4 GB to 32 GB	2 GB to 32 GB	4 GB to 16 GB	4 GB to 16 GB
Speed up to (MT/s)	3200	3200	3200	3200	3200	2400	2400
PCB Height*	Low profile / VLP / ULP	Low profile / VLP / ULP	Low profile / VLP / ULP	Low Profile	Low Profile	Low profile / VLP / ULP	Low profile / VLP / ULP
Operating Temperature (Ta)	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C	0°C to 85°C / -40°C to 85°C

* VLP: 0.74", ULP: below 0.74"

Please refer to motherboard/CPU/chipset documentation for memory requirements and compatibility.

DDR5

DDR5 is the next-generation DRAM specification. It is poised to exceed DDR4 in every way. DDR5 promises faster performance, higher memory bandwidth, higher densities, and a new power management structure that delivers better power efficiency. All of these advantages, and more, are expected to meet the ever-growing memory needs of present and future applications.

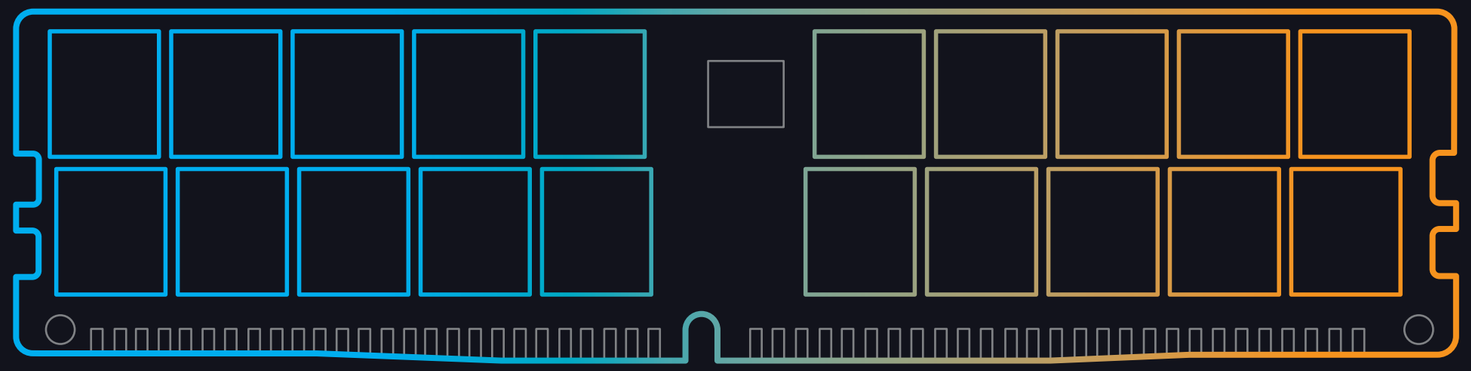
Both DDR4 and DDR5 dual-inline memory modules (DIMMs) still have 288 pins, but with DDR5's higher bandwidth, this means it can transmit data faster. While the pin count is the same, DDR5 DIMMs will not fit in DDR4 sockets as the alignment key is located differently and the pinouts have been changed to accommodate the new features.

Up to
6.4 Gbps
Memory Bandwidth

4800 to 6400 MHz
Frequency / Transfer Rate

Per die
Up to 64 Gb
Memory Density

1.1V
Operating Voltage



DDR5 Advantages Over DDR4

Memory Bandwidth

This refers to the theoretical maximum amount of data that can be transmitted (read/written) within a given time. Memory bandwidth is expressed in gigabits per second (Gbps). DDR5 memory bandwidth is initially at 4.8 Gbps per pin, compared with DDR4's 3.2 Gbps. Future versions are expected to double DDR4's, going up to a maximum of 6.4 Gbps.

Frequency / Transfer Rate

Memory frequency refers to the number of commands or transfer operations that the memory module can handle per second. It is typically expressed in megahertz (MHz), but some manufacturers use express this in mega transfers per second (MT/s). The number follows the DDR version, so a DDR5-4800 DIMM, for example, has a frequency of 4800 MHz (or 4800 MT/s).
DDR4 frequency ranges from 1866 to 3200 MHz, while DDR5 ranges from 4800 to 6400 MHz initially, but may go as high as 8400 MHz.

Memory Density

DDR4 maximum density is 16 Gb per die, so with 16 die, this translates to 256 Gbit or a total of 32 GB. DDR5, in comparison, has 64 Gb per die, translating to 1024 Gbit or a total of 128 GB – this is 4X that of DDR4, enabling higher-capacity DIMMS!

Burst Length

This is the amount of data, which is input/output based on a single read/write command in DRAM.
DDR5 doubles DDR4 burst length from 8 to 16, thus increasing the read/write efficiency.

Power Management and Consumption

The first power management IC (PMIC) on DIMM is introduced in DDR5. PMIC performs local voltage regulation on the module. Historically, voltage regulation has been done on the motherboard. PMIC on the module allows additional features such as threshold protection, error injection capabilities, programmable power-on sequence, and power management features (Source: Micron). DDR5's lower voltage of 1.1V compared with DDR4's 1.2V further reduces power consumption.

DDR5 vs. DDR4

The following table summarizes important enhancements of DDR5 from DDR4.

	DDR5	DDR4
VDD*	1.1V	1.2V
Data Rates	4800 to 6400 MT/s	1866 to 3200 MT/s
Component Density	16 Gb to 64 Gb	4 Gb to 16 Gb
DQ Bus Width (NON-ECC/ECC)	64/80 bits	64/72 bits
On-Die ECC	Yes	No
Power Management	On DIMM PMIC*	On Motherboard

* VDD: Stands for Voltage Drain Drain, which is the drain power voltage
PMIC: Power Management Integrated Circuit

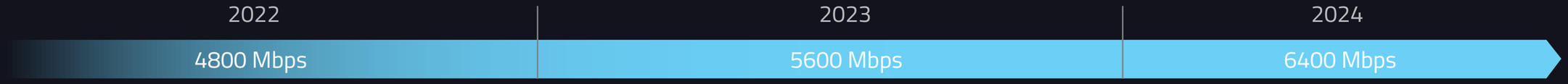
DDR5 Market Situation

While many module houses started sampling 1st Gen. DDR5 to customers in 2021, the price gap at the functional level to justify the adoption for DDR5 over DDR4 is too wide to consider in ATP's view.

DDR5 vs. DDR4		
	DDR4	DDR5
8 GB UDIMM	1x	1.57x
DDR5 Component	1x	1.7x

Insider Tips on Time-to-Market for DDR5

- DDR5 timeframe
  - Price is key. Future die shrink and optimizer will lead to a better commercial situation for DDR5 adoption

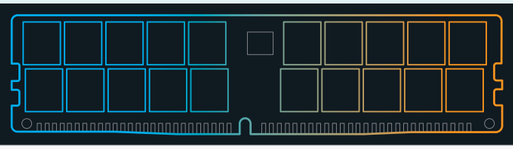


DDR5 ecosystem starts to build up:
- 1st usage will be consumer applications
- CM/EMS start to develop relevant platforms to be on AVL
- Servers will release 1st Gen to support DDR5

- Speed will be upgraded to 5600 MT/s.
- DDR5 will be the primary focus of NPIs.
- DDR5 is still premium but gap may minimize between 15-20%.

Sweet spot for DDR5 products

Summary: DRAM Generations

		Generation	Voltage	Pin Count
TSOP II Package		SDRAM	3.3V	168 pins
		DDR1	2.5V	184 pins
BGA Package		DDR2	1.8V	240 pins
		DDR3	1.5V / 1.35V	240 pins
		DDR4	1.2V	288 pins
		DDR5	1.1V	288 pins

Categories

Categories by Form Factor

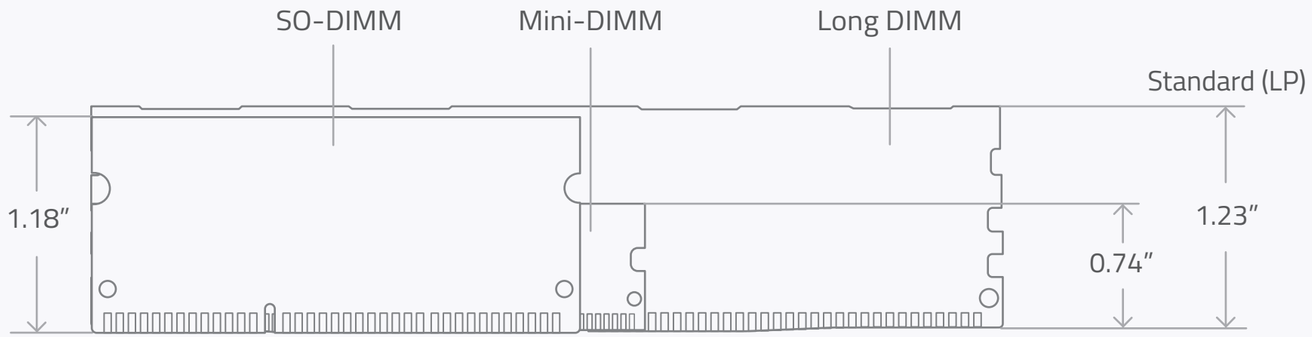
Length

- Long DIMM
- SO-DIMM*
- Mini-DIMM

Height

- Standard (LP): 1.18″ to 1.23″
- VLP*: 0.72″ to 0.74″
- ULP*: 0.7″ to 0.72″

Form factor dimensions may vary depending on DRAM generation. The illustration below shows the height of different DDR4 form factors.



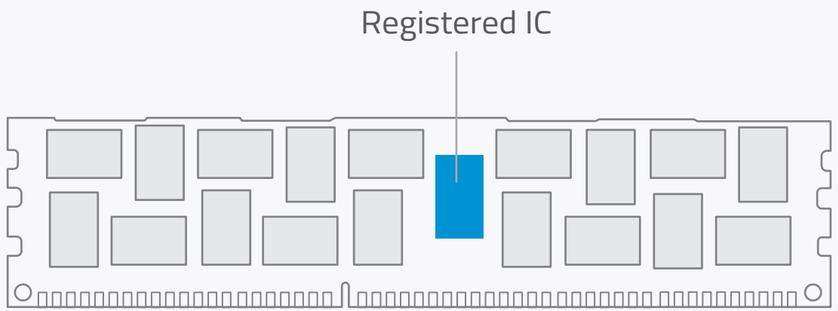
DDR4 DRAM heights by form factor

* SO-DIMM: Small Outline Dual In-Line Memory Module
  VLP: Very Long Profile
  ULP: Ultra Low Profile

Categories by Function

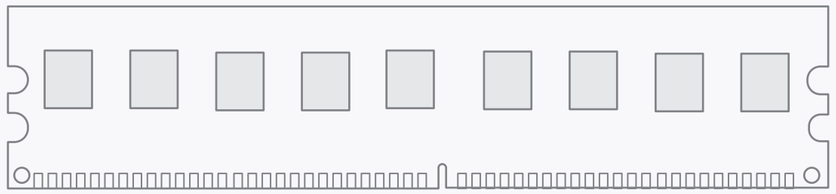
RDIMM (Registered)

- Also known as "buffered" memory, RDIMMs feature onboard memory registers (hence the name "registered") placed between the memory and the system's memory controller.
- The register controls the amount of control and address signals that flow onto the module.
- The memory controller buffers Command, Addressing and Clock Cycling, directing instructions to the dedicated memory registers instead of accessing the DRAM directly. This reduces the electrical load on the memory controller.



UDIMM (Unbuffered/Unregistered)

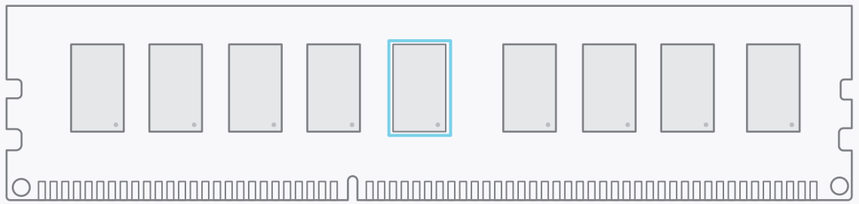
- Used mainly on consumer desktop and laptop computers, they run faster and cost less but are not as stable as registered memory. Commands go directly from the memory controller residing in the CPU to the memory module.
- The chipset of system drive directly controls and addresses signals into the memory chips of the module without any logical chips between chipset and memory chips.



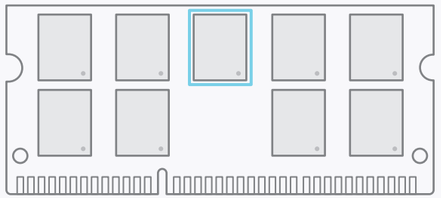
Categories by Function

Error Correction Code (ECC) DIMM

- An ECC memory module has an additional memory chip to detect and correct errors.
- ECC DIMMs typically have 9 or 18 memory chips to realize a module data width of 72 bits.



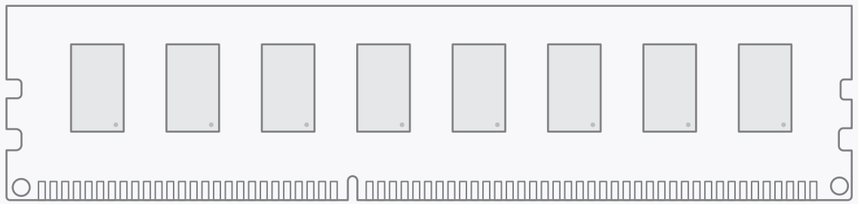
ECC UDIMM



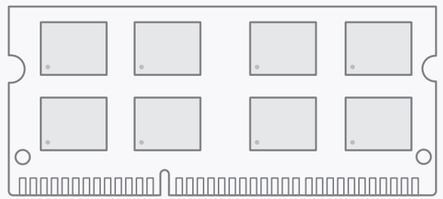
ECC SO-DIMM

Non-ECC DIMM

- Non-ECC modules have either 8 or 16 DRAM components to realize a module data width of 64 bits.



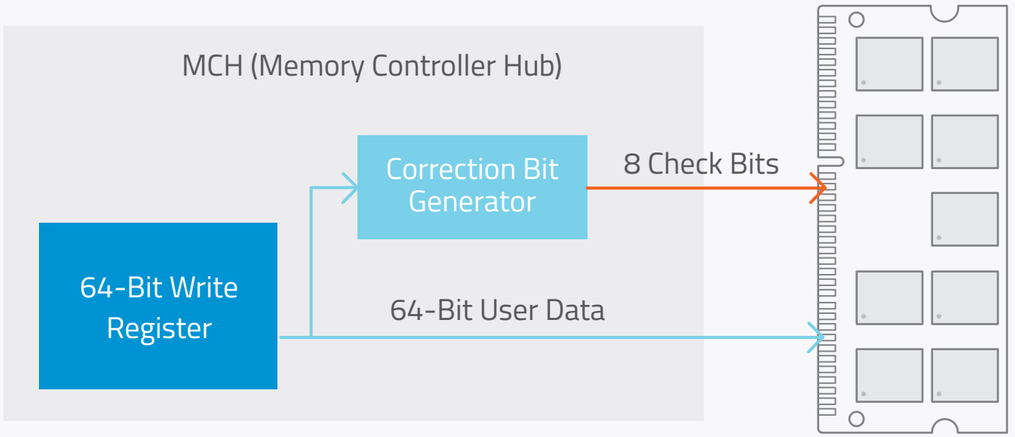
Non-ECC UDIMM



Non-ECC SO-DIMM

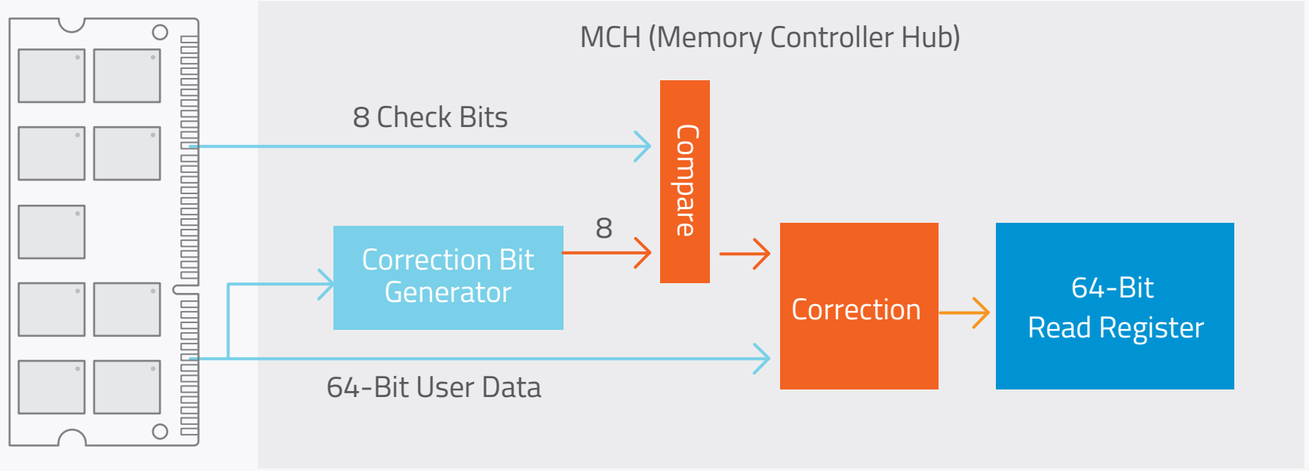
Implementation of ECC Writes

- The error correction is performed in the MCH (Memory Controller Hub) alone.
- The DRAM module has a data width of 72 bits and all ECC codes will not modify the 64-bit user data.
- The correction bit generator will create 8 check bits by computing different checksums out of the 64 bits.
- The 64-bit user data and 8 check bits are written in parallel into the module.



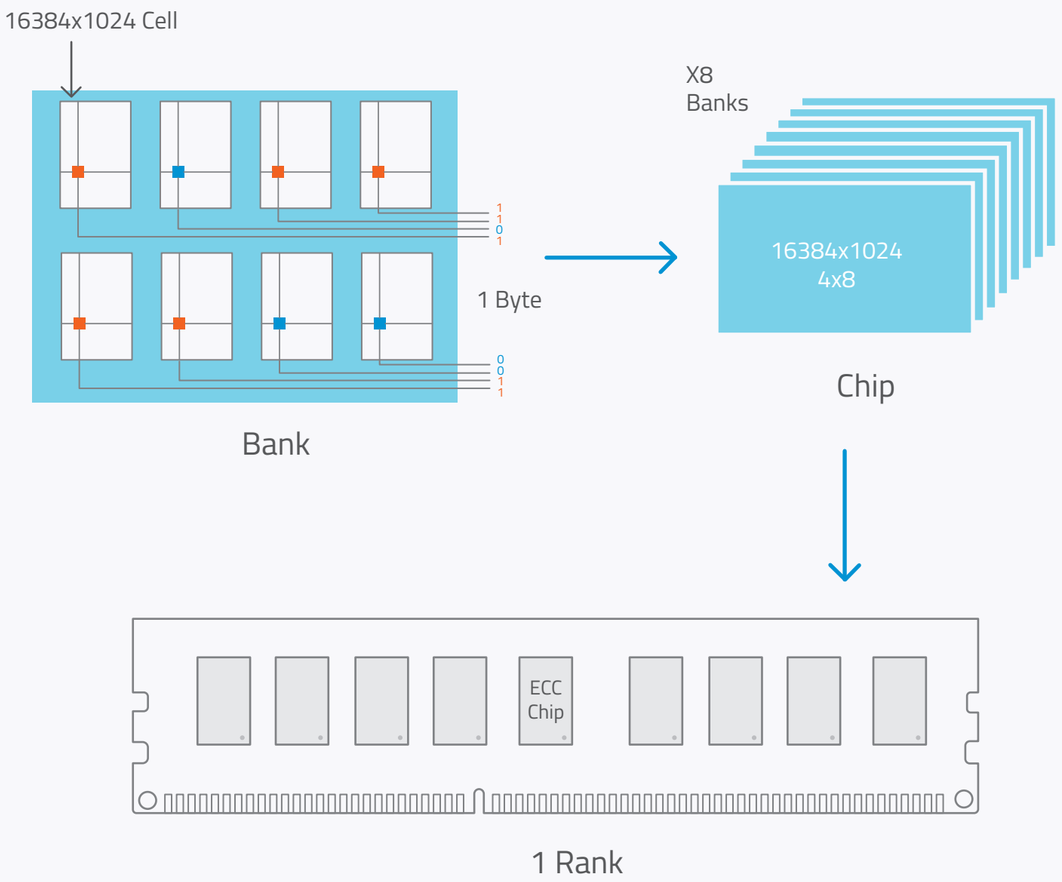
Implementation of ECC Reads

- A read from the module provides 72-bit data, 64-bit user data and 8 check bits
- The correction bit generator creates a “new” set of 8 check bits.
- The read check bits and a new set are compared
  - If equal → no failure
  - If not equal → bit error
  - Comparison results indicate wrong bit position
- Inversion unit fixes the wrong bit and correct data is transferred to the read register



Module Organization and Capacity

Side/Rank/SPD



- **Bank**
  - A set of memory arrays is called a Bank.
  - Data width of a Bank: 4/8/16 bits
- **Chip**
  - Only one bank can be accessed each time.
    ⟶ Chip data width = Bank data width
- **Rank**
  - A set of chips forms a Rank.
    1 Rank = 64-bit / 72-bit (ECC).
  - Each rank works independently and has its own chip selection signal: CS. Following JEDEC standard, DDR4 can have 1, 2, or 4 ranks.

Side/Rank/SPD

Double-Sided

It is a physical term that means memory chips are located on two sides of the memory module.

Dual Rank

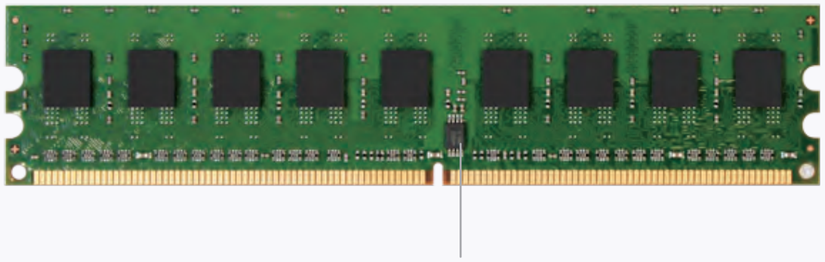
It is an electrical term that means the module is divided electrically into two memory ranks.

1 Rank = 64 bits (Non-ECC) / 72 bits (ECC)

The physical arrangement of the chips does not always indicate the rank. Single-sided modules may not always be a single rank, and dual-sided modules may not always be dual rank.

Serial Presence Detect (SPD)

- SPD uses an E^2PROM (also called EEPROM) to store information on the configuration of memory modules, such as timing parameters, manufacturer, serial number and other useful information about the module.
- E^2PROM stands for “electrically erasable programmable read-only memory.” It is a type of non-volatile memory that stores a small amount of data. It allows users to erase and reprogram an individual byte of stored data using electrical voltage.



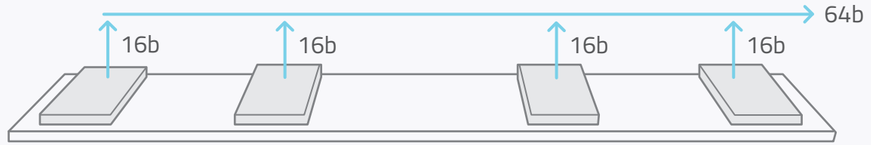
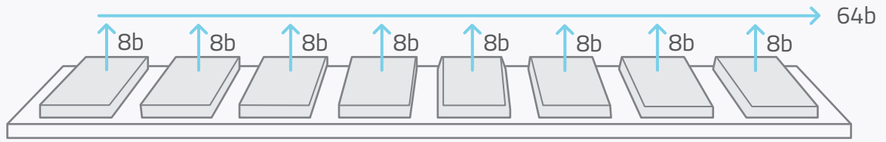
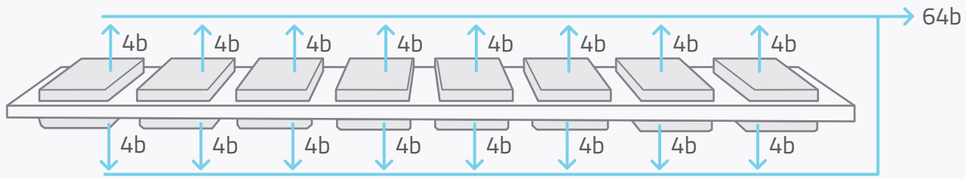
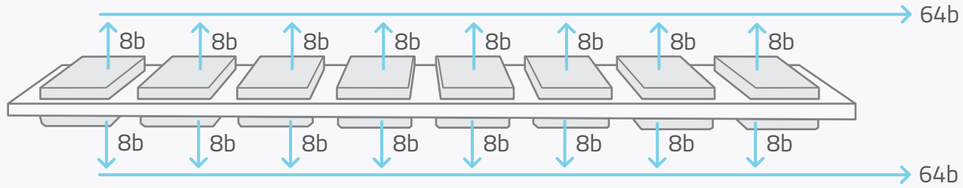
Chip Density and Configuration

Chip density refers to the amount of memory cells of an individual chip on the module.
The following table shows typical chip densities and configurations.

Chip Density & Configurations		Address Mapping	Data Width
4 Gb	1024 Mb x 4	1024 Mb	4 bits
	512 Mb x 8	512 Mb	8 bits
	256 Mb x 16	256 Mb	16 bits
8 Gb	2048 Mb x 4	2048 Mb	4 bits
	1024 Mb x 8	1024 Mb	8 bits
	512 Mb x 16	512 Mb	16 bits
16 Gb	4096 Mb x 4	4096 Mb	4 bits
	2048 Mb x 8	2048 Mb	8 bits
	1 Gb x 16	1024 Mb	16 bits

Module Rank and Capacity Calculation

1 Rank = Data width of 64 bits (72 bits if with ECC)

1Rx16	1 rank with four pcs. 16-bit wide chips on one side		Single Rank
1Rx8	1 rank with eight pcs. 8-bit wide chips on one side		Single Rank
1Rx4	1 rank with 16 pcs. 4-bit wide chips on two sides, for a total of 16 pcs.		Single Rank
2Rx8	2 ranks with 16 pcs. 8-bit wide chips on two sides, for a total of 16 pcs.		Dual Rank

Capacity Calculation

How to compute module capacity

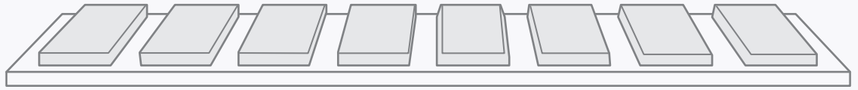
Sample IC/component capacity: 8 Gb

Notes: 1 GB* = 8 Gb*
ECC ICs are not included in the capacity calculation

Formula: IC Capacity x Pcs. of IC / 8 bits = Module Capacity

8 Gb x 4 pcs./8 bits = **4 GB**

8 Gb x 8 pcs./8 bits = **8 GB**



8 Gb x 16 pcs./8 bits = **16 GB**

8 Gb x 16 pcs./8 bits=**16 GB**

*GB: Gigabyte
**Gb: Gigabit

Applications

RDIMM/LRDIMM

Data Center:
Maximized utilization and quick scale-out performance

Cloud:
High density, low power solutions improve TCO

UDIMM/SODIMM

Micro Server: Low cost and reduced latency

Embedded: Wide range of capacity options

Chapter 2
ATP Differentiators

Industrial Quality

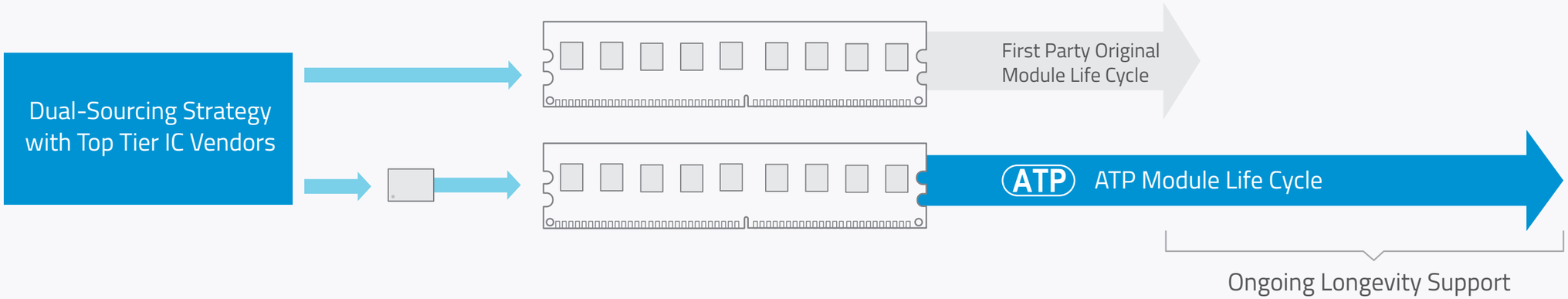
ATP is committed to providing the highest-quality DRAM modules suitable for rigorous industrial and embedded applications.

- Designed and manufactured with extensive screening & testing
- Best TCO value with longevity & higher endurance for industrial applications
- Full in-house process ownership for uncompromising quality guarantee

The ATP quality umbrella covers both mainstream original modules and second-source/legacy ATP-built modules.

Whole Project Life Cycle ATP QA + Traceability

- Coverage of multiple DRAM suppliers and process nodes
- BOM Control, Label traceability
- ATP Quality/Testing Coverage



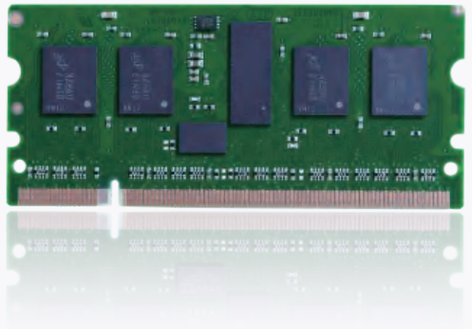
Longevity Program

Micron and ATP Partnership and License Agreements ensure legacy DDR2/DDR/SDR DRAM module supply.

DDR2 Continuity Program

With DDR2 still widely deployed in the US, Japan and Europe, ATP and Micron are making sure that these markets will have a steady supply of Micron DDR2 SO-DIMMs and UDIMMs for industrial/embedded systems installed in high-reliability and mission-critical environments. All modules are manufactured, tested and validated by ATP, according to the equivalent specifications and testing/validation processes of the respective Micron part number.

Module Type	DDR2 UDIMM	DDR2 SO-DIMM
Capacity	1 GB / 2 GB	256 MB / 1 GB / 2 GB / 4 GB
Function	Unbuffered ECC / Unbuffered Non-ECC	Unbuffered Non-ECC
Frequency	800 MHz	800 MHz
Number of Pins	240	200
PCB Height	1.18"	1.18"



Longevity Program

Legacy (SDR/DDR) DRAM Modules

Under a license agreement with Micron Technology, Inc. signed in August 2015, ATP will continue to manufacture legacy SDR/DDR DRAM modules for Micron's customers who are unable to migrate. The agreement was expanded in 2016 with the addition of selected legacy DRAM modules specifically for customers using AMD Embedded/Geode platforms. ATP works closely and exclusively with Micron to transfer module designs and extend long-term support to offer the legacy modules in selected form factors (SO-DIMM, UDIMM and RDIMM) and densities, along with ATP's unique services and features.

The license agreement stipulates the following conditions for ATP:

- 100% follow Micron's design. Offer extended support for these legacy products to minimize the customer's (re)qualification efforts.
- 100% follow Micron's BOM selection. Implement the same specifications for key components (such as IC configuration and Register/PLL type), as well as passive components (such as resistors, capacitors and EEPROM) to meet the specifications of Micron's BOM.
- 100% follow Micron's firmware settings. Implement SPD in addition to the manufacturer's information.
- 100% follow Micron's specifications. Each module will be manufactured to the equivalent specifications and test processes of the corresponding Micron part number.

Longevity Program

Product Information

Module Type	Capacity	Function	Frequency	Number of Pins	PCB Height
DDR SO-DIMM	128 MB / 256 MB / 512 MB / 1 GB	Unbuffered Non-ECC	400 MHz	200	1.25"
DDR SO-DIMM (Industrial Grade)	256 MB / 512 MB	Unbuffered Non-ECC	400 MHz	200	1.25"

Build To Order (BTO)					
Module Type	Capacity	Function	Frequency	Number of Pins	PCB Height
DDR UDIMM	256 MB / 512 MB	Unbuffered Non ECC	400 MHz	184	1.25"
SDRAM SO-DIMM	64 MB / 128 MB / 256 MB	Unbuffered Non ECC	133 MHz	144	1.0" / 1.25"

ATP DRAM Testing

ATP DRAM modules undergo two levels of stringent Enhanced Module-Level Tests.
Automatic Test Equipment (ATE) and system-level Test During Burn-In (TDBI) guarantee that modules meet and even exceed qualifying parameters.

FUNCTIONAL/ATE TESTING	SYSTEM TESTING
▪ Detects structural and component defects ▪ Screens out marginal timings/SI sensitivities	▪ 100% System-level burn-in testing ▪ 100% TDBI* accelerated burn-in testing effectively Screens out weak ICs

*Test During Burn-In. On a project basis; value-added service.

ATP DRAM Testing

FUNCTIONAL/ATE TESTING

1. Automatic Test Equipment (ATE)

2. Load SPD

SYSTEM TESTING

TDBI: Testing During Burn In

- Room Temperature : SDRAM/DDR/DDR2/DDR3/DDR4
- Industrial/Wide Temp (-40°C to 85°C):
  - DDR2
  - DDR3
  - DDR4

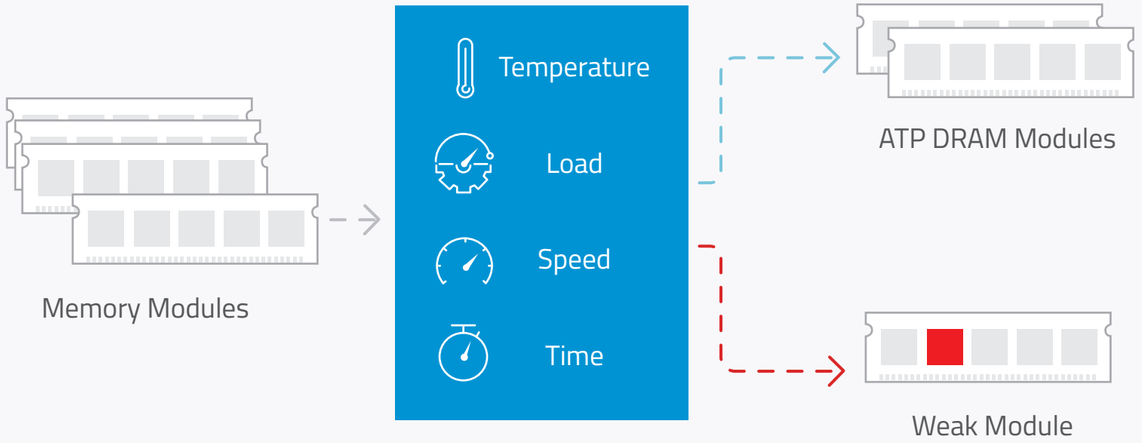
ATP DRAM Testing

Automatic Test Equipment (ATE)

The ATE detects component defects and structural defects related to the DIMM assembly and screens out marginal timing and signal integrity (SI) sensitivities. ATE provides electrical testing patterns with various parameter settings, such as marginal voltage, signal frequency, clock, command timing and data timing under continuous thermal cycle.

Test During Burn-in (TDBI)

- TDBI at mass production level detects early life failures (ELF) and effectively screens out weak ICs that could fail during the early product life. It combines temperature, load, speed and time to stress test memory modules and expose the weak module.
- Even just 0.01% error on a 99.99% effective device can increase the failure rates at module level and lead to failure in actual usage.
- ATP TDBI can detect and screen out the 0.01% error to ensure utmost reliability.

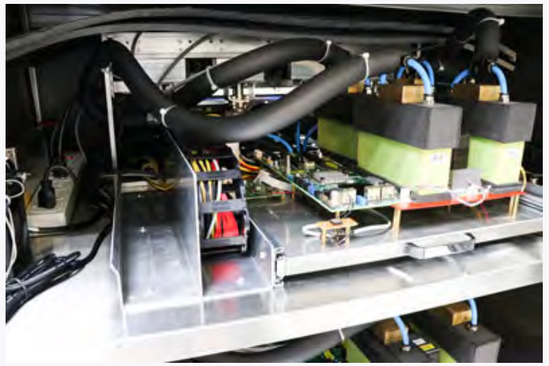


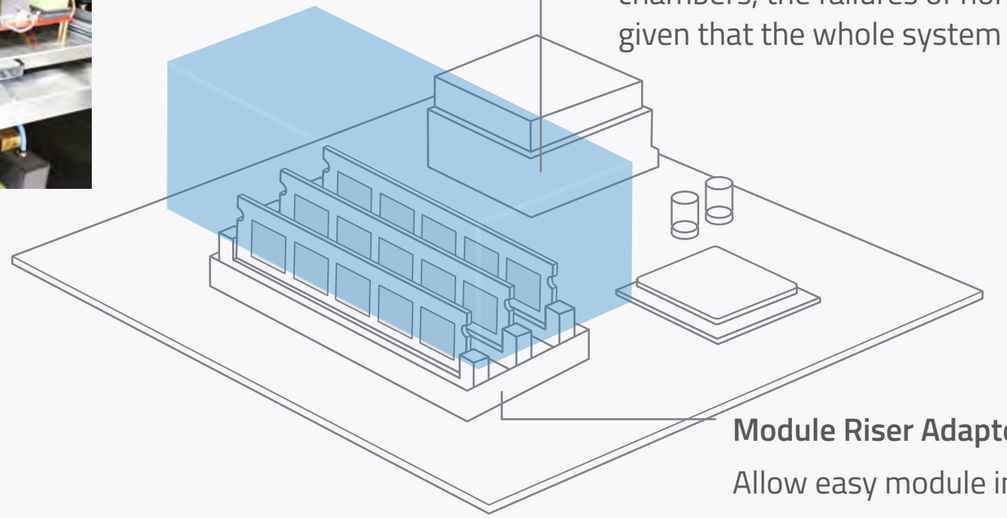
ATP DRAM Testing

ATP TDBI: What Makes It Unique?

The ATP TDBI system applies extreme high/low temperature, high-low voltage, and pattern testing on DRAM modules.

The system consists of:





The Mini Chamber

Isolates temperature cycling only to modules being tested so as not to thermally stress the rest of testing systems. This minimizes the failure of other testing components, such as the motherboards. It also allows faster debug for defects per million (DPM) fallout and reduced false failures. In conventional large thermal chambers, the failures of non-DRAM-related testing components are constant, given that the whole system is thermally stressed.

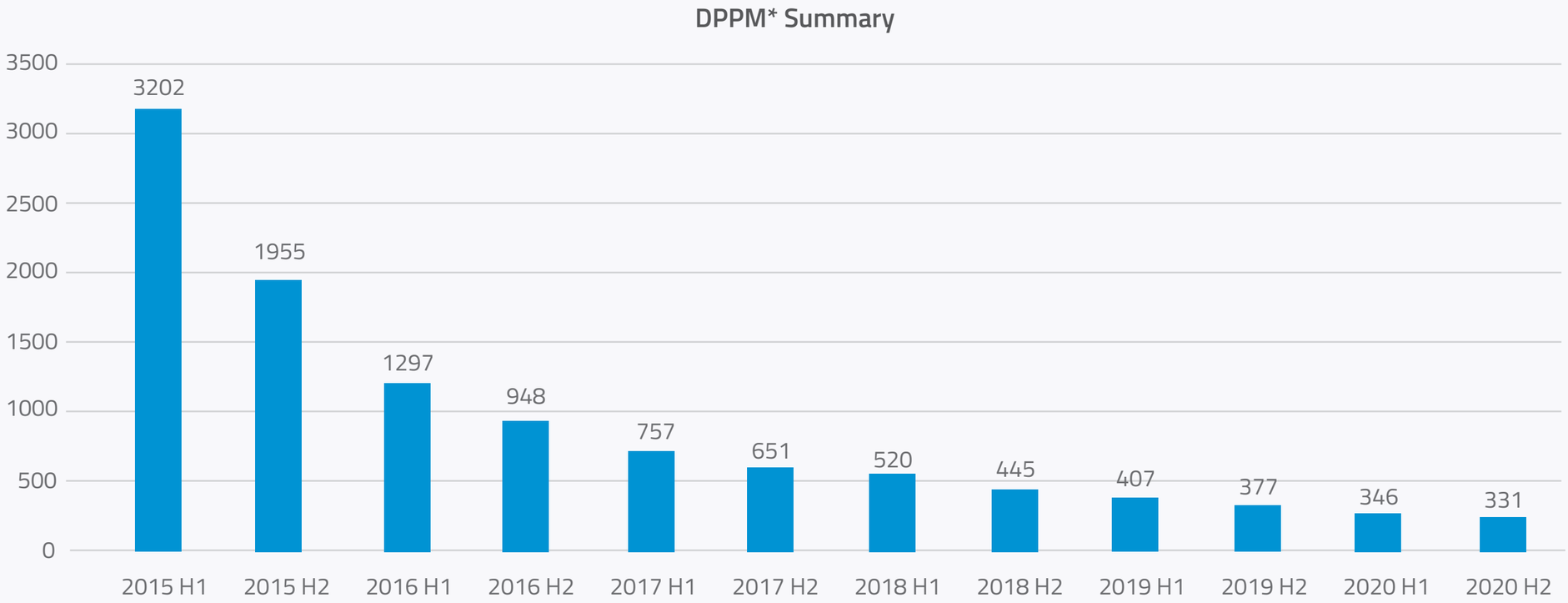
Module Riser Adapters from the Motherboard

Allow easy module insertions in production-level volumes.

ATP DRAM Testing

Improvements After TDBI Adoption

The following graph shows that with ATP TDBI, the error rates decrease over time. The acceptable industry limit is 3,500 DPPM,* but with ATP TDBI, the error rate has gone down to just over 100 during the fourth year.

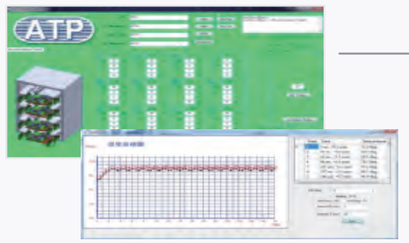


*DPPM = Defective Parts per Million

ATP DRAM Testing

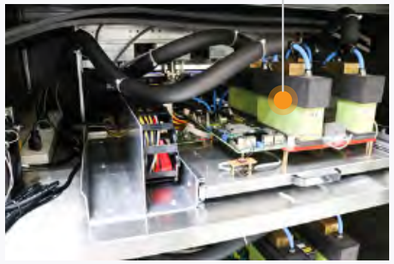
ATP TDBI Equipment Overview

High/Low Temp Validation
(-40°C to 85°C)



1 Cabinet

carries **4** motherboards



Mini Chambers

Other Unique Features

Wide Temp DRAM Modules

Industrial grade modules can cost up to 2.5 times higher than commercial grade modules. ATP offers wide temperature modules, which can offer the best solution to reach industrial grade performance at a lower cost.

	Commercial Grade Modules	Wide Temperature Modules	Industrial Grade Modules
Target Market	General DRAM Product	Price Issue with IG Solution	Customer-Specified
DRAM IC	Major IC	Wide Temp IC	Native IG* IC
Operating Temp	0°C to 85°C	-40°C to 85°C	-40°C to 85°C
Testing Feature	ATE & Module Level TDBI	ATE & Module Level Enhanced TDBI (-40°C to 85°C)	ATE & Module Level TDBI
Cost	1x$	$CG* < $WT* DRAM < $IG*	2.5 X $

*WT: Wide Temperature
IG: Industrial Grade
CG: Commercial Grade

Other Unique Features

30μ" Golden-Plated Connector

In order to achieve the best durability, all ATP DRAM modules comply with IPC-A-610 and adopt a 30μ (micro-inch) golden-plated connector to ensure stability under any tough environment.

The 30μ"-thick gold plating of the DRAM contact optimizes signal transmission quality between the connector and the DRAM module.

Anti-Sulfur Resistors*

Ordinary silver resistors corrode and become non-conductive when exposed to sulfur. ATP DRAM modules products offer an anti-sulfur resistor option to prevent the corrosive effects of sulfur contamination, guaranteeing continued dependable performance for a long time and lowering the total cost of ownership by preventing unnecessary downtime and expensive component replacements.

* Value-added feature, by project support.

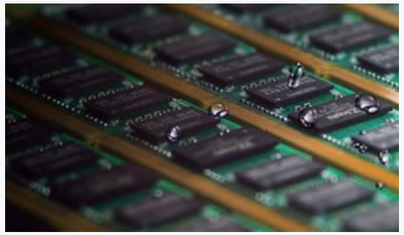
Customization Services

Depending on customer request, ATP offers optional value-added services.

Conformal Coating

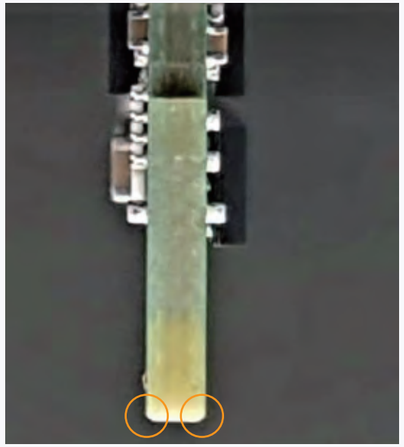
Dust, chemical contaminants, extreme temperatures and moisture, corrosion may lead to DRAM short circuiting and malfunction.

ATP uses conformal coating to protect against contaminants and increase the DRAM modules' service life. ATP's conformal coating solution uses parylene coating technology via chemical vapor deposition (CVD). The coating material, which is compliant with US Military Material MIL-I-46058C and Fire Safety UL94V-0 Certification standards, is placed in a vacuum chamber. Inside the chamber, the coating material is directly vaporized and pyrolyzed into nano-molecular streams. It is then entered into a room-temperature coating chamber to gradually form an even and homogeneous protective film onto the profile of the DRAM module circuit assembly. The coating completely penetrates spaces as narrow as 0.01 mm, making it totally pinhole-free and truly conformal to shield the DRAM module from dust, chemicals, moisture, and other harmful substances.



Chamfering PCB Design

Chamfering refers to the process of "beveling or tapering" the connector edges for easier insertion into the memory slots. The bevel is done at specific angles, typically at around 40° to 50°.



ATP DRAM Products

Complete DRAM Portfolio

Product	DIMM Type	Capacity	Speed (MT/s, up to)	VLP/ULP*	30μ" Golden Finger	ATP TDBI	Wide Temperature	Anti-Sulfur Resistors	Conformal Coating	PCB Chamfer
DDR4	RDIMM	4 GB to 128 GB	3200	●	●	●	▲	▲	-	▲
	ECC UDIMM	4 GB to 32 GB	3200	●	●	●	▲	▲	▲	▲
	Non-ECC UDIMM	2 GB to 32 GB	3200	●	●	●	▲	▲	▲	▲
	ECC SO-DIMM	4 GB to 32 GB	3200	-	●	●	▲	▲	▲	▲
	Non-ECC SO-DIMM	2 GB to 32 GB	3200	-	●	●	▲	▲	▲	▲
	Mini-RDIMM	4 GB to 16 GB	2400	●	●	●	▲	▲	-	-
	Mini-UDIMM	4 GB to 16 GB	2400	●	●	●	▲	▲	-	-

▲ : Optional
* VLP : height = 0.74"
ULP : height below 0.74"

Complete DRAM Portfolio

Product	DIMM Type	Capacity	Speed (MT/s, up to)	VLP/ULP*	30μ" Golden Finger	ATP TDBI	Wide Temperature	Anti-Sulfur Resistors	Conformal Coating	PCB Chamfer
DDR3	RDIMM	1 GB to 32 GB	1866	●	●	●	▲	▲	-	▲
	ECC UDIMM	1 GB to 16 GB	1866	●	●	●	▲	▲	▲	▲
	Non-ECC UDIMM	1 GB to 16 GB	1866	●	●	●	▲	▲	▲	▲
	ECC SO-DIMM	1 GB to 16 GB	1866	-	●	●	▲	▲	▲	▲
	Non-ECC SO-DIMM	1 GB to 16 GB	1866	-	●	●	▲	▲	▲	▲
	Mini-RDIMM	1 GB to 16 GB	1600	●	●	●	▲	▲	-	-
	Mini-UDIMM	1 GB to 16 GB	1600	●	●	●	▲	▲	-	-

▲: Optional
* VLP: height = 0.74"
ULP: height below 0.74"

Complete DRAM Portfolio

Product	DIMM Type	Capacity	Speed (MT/s, up to)	VLP/ULP*	30μ" Golden Finger	ATP TDBI	Wide Temperature	Anti-Sulfur Resistors	Conformal Coating	PCB Chamfer
DDR2	ECC UDIMM	1 GB to 2 GB	800	-	●	●	▲	-	-	-
	Non-ECC UDIMM	1 GB to 2 GB	800	-	●	●	▲	-	-	-
	Non-ECC SO-DIMM	256 MB / 1 GB to 4 GB	800	-	●	●	▲	-	-	-
DDR1	Non-ECC UDIMM	256 MB	400	-	●	●	-	-	-	-
	Non-ECC SO-DIMM	128 MB to 512 MB / 1 GB	400	-	●	●	▲	-	-	-
SDRAM	Non-ECC SO-DIMM	64 MB to 256 MB	PC 133	-	●	●	-	-	-	-

▲ : Optional
* VLP : height = 0.74"
ULP : height below 0.74"

Ordering Information

Hot Items Ordering Information							
Product	DIMM Type	Speed (MT/s, up to)	SIZE	CHIP	HEIGHT	Ranks	P/N
DDR3	Unbuffered Non ECC UDIMM	1600	4 GB	512x8	1.18"	1	AQ12P64A8BLK0M
	Unbuffered Non ECC UDIMM	1600	8 GB	512x8	1.18"	2	AQ24P64B8BLK0M
	Unbuffered Non ECC SO-DIMM	1600	4 GB	512x8	1.18"	1	AW12P6438BLK0M
	Unbuffered Non ECC SO-DIMM	1600	8 GB	512x8	1.18"	2	AW24P64F8BLK0M

Hot Items Ordering Information							
Product	DIMM Type	Speed (MT/s, up to)	SIZE	CHIP	HEIGHT	Ranks	P/N
DDR4	Unb/Non ECC SO-DIMM	3200	4 GB	512x16	1.18"	1	A4G04QC6BNWE*O
		3200	8 GB	1Gx16	1.18"	1	A4G08QC6BVWE*O
		3200	16 GB	2GX8	1.18"	1	A4G16QA8BVWE*O
		3200	32 GB	2GX8	1.18"	2	A4G32QE8BVWE*O
	Unb/Non ECC SO-DIMM	2666	4 GB	512x16	1.18"	1	A4G04QC6BNTD*O
		2666	8 GB	1Gx16	1.18"	1	A4G08QC6BVTD*O
		2666	16 GB	2GX8	1.18"	1	A4G16QA8BVTD*O
		2666	32 GB	2GX8	1.18"	2	A4G32QE8BVTD*O

* M= Micron-based module, S= Samsung-based module

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